

MODEL NAME : **VAUB0**

PCB NO : **LA-9941P**
DAA0006W000

BOM P/N : **TBD**

Dell/Compal Confidential

Schematic Document

Phantom (Shark Bay)

Haswell (BGA) + Lynx Point

DISCRETE VGA N14P (optimus) --- Testarossa
DISCRETE VGA N15P (optimus) --- Testarossa-P

2013-01-02

Rev: 0.1 (X00)

@ : Nopop Component

CONN@ : Connector Component

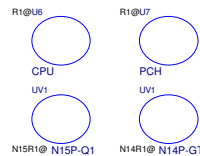
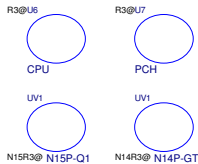
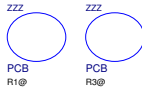
TPM@ : TPM function

DSP@ : DSP function

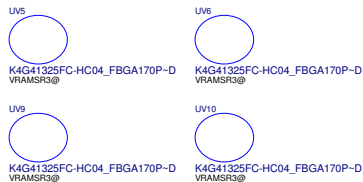
N14@ : DGPU N14P-GT

N15@ : DGPU N15P-Q1

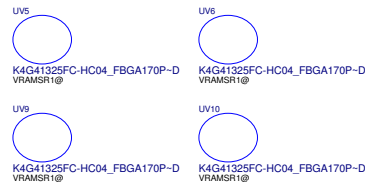
www.aitech1.ru



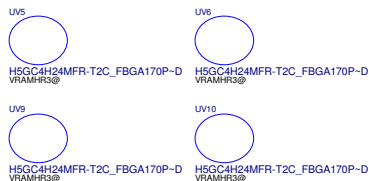
Samsung 2G



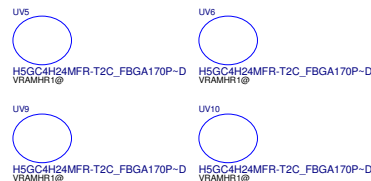
Samsung 2G



Hynix 2G



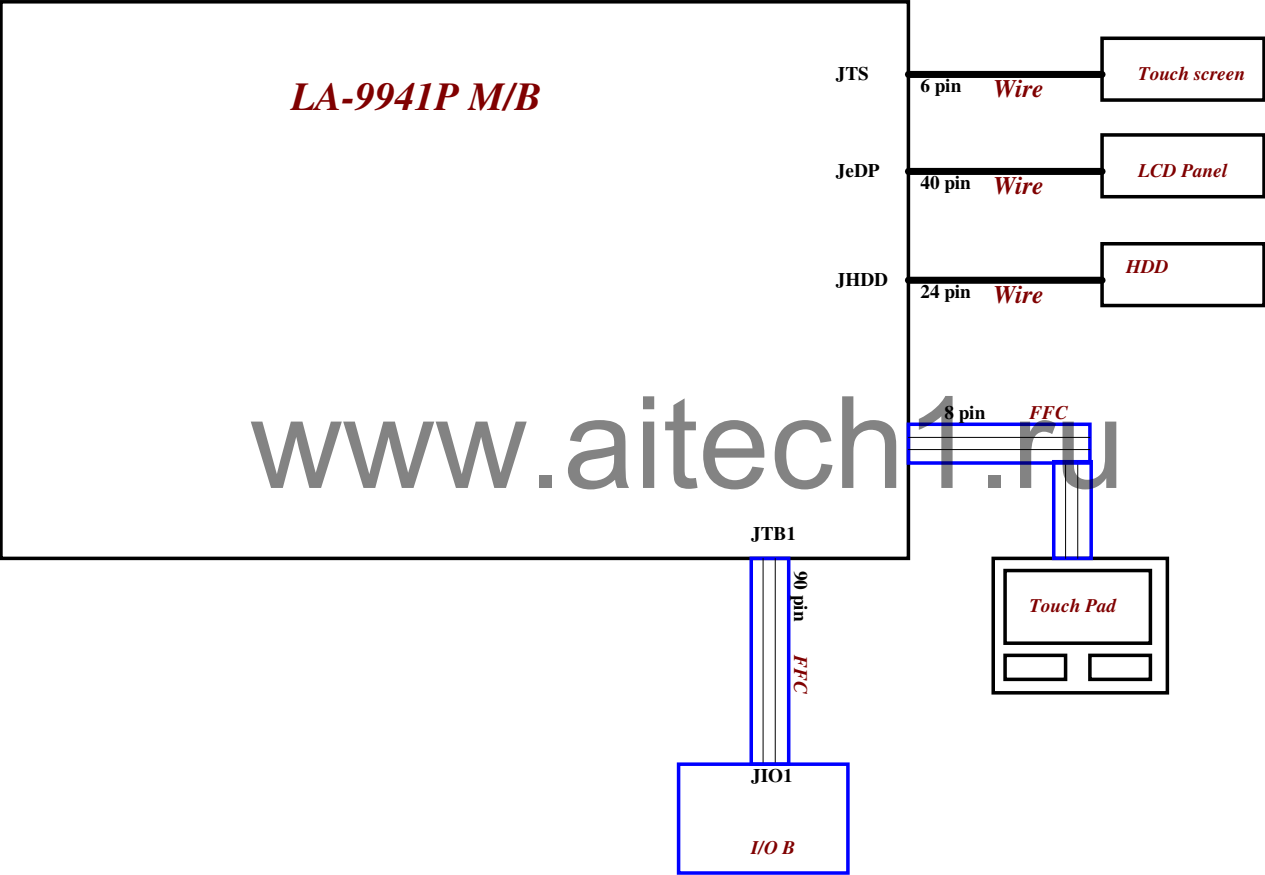
Hynix 2G



Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2011/08/25	Document Number	LA-7851P	Rev 0.1
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.						
Date: Wednesday, September 04, 2013				Sheet	1	of 62

Compal Confidential

Project Code : VAUB0
File Name : LA-9941P



Vcc	3.3V				
Ra	100K +/- 1%				
Board ID	Rb		Board ID	PCB Revision	
0	0		0	DIS 0.1	
1	12K +/- 1%		1	DIS 0.2	
2	15K +/- 1%		2	DIS 0.3	
3	20K +/- 1%		3	DIS 0.4	
4	27K +/- 1%		4	DIS 0.5	
5	33K +/- 1%		5	DIS 1.0	
6	43K +/- 1%		6	DIS-P 0.2	
7	56K +/- 1%		7	DIS-P 0.3	
8	75K +/- 1%		8	DIS-P 0.4	
9	100K +/- 1%		9	DIS-P 1.0	
10	130K +/- 1%		10	UMA 0.2	
11	160K +/- 1%		11	UMA 0.3	
12	200K +/- 1%		12	UMA 0.4	
13	240K +/- 1%		13	UMA 1.0	
14	270K +/- 1%		14		
15	330K +/- 1%		15		
16	430K +/- 1%		16		
17	560K +/- 1%		17		
18	750K +/- 1%		18		
19	NC		19		

PCI EXPRESS	DESTINATION
Lane 1	None
Lane 2	None
Lane 3	MINI CARD-1 WLAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

SATA	DESTINATION
SATA0	HDD
SATA1	SSD
SATA2	None
SATA3	None
SATA4	None
SATA5	None

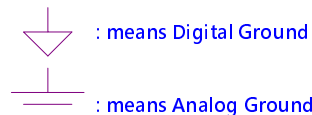
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC LPC
PCI2	None
PCI3	None
PCI4	None

	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
CLK	CLKOUT_PCIE0	None	CLKOUTFLEX0	CLK_PCI_TPM
	CLKOUT_PCIE1	None	CLKOUTFLEX1	None
	CLKOUT_PCIE2	None	CLKOUTFLEX2	None
	CLKOUT_PCIE3	MINI CARD-1 WLAN	CLKOUTFLEX3	None
	CLKOUT_PCIE4	CARD READER		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
	CLKOUT_PEG_B	None		

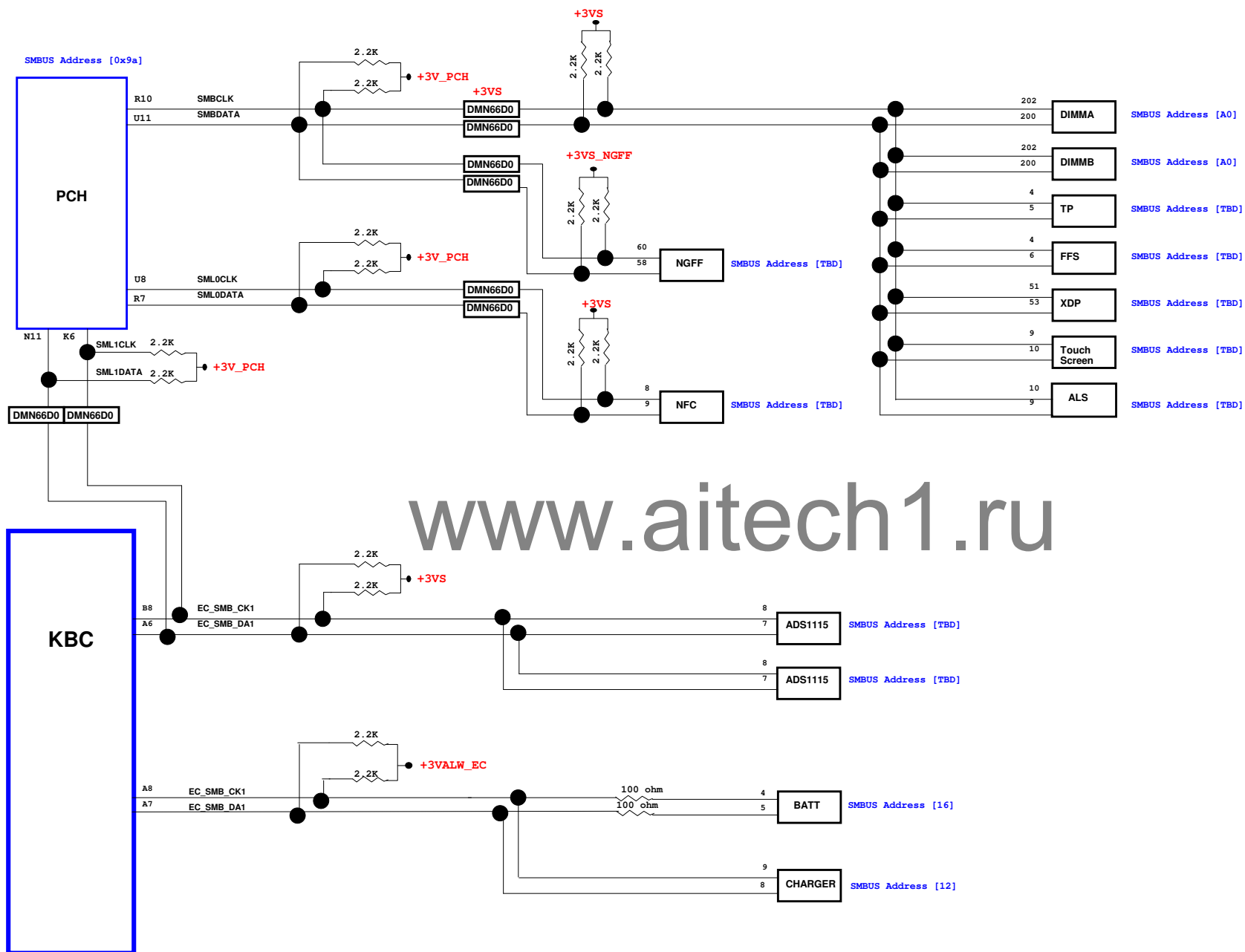
PCH	USB PORT#	DESTINATION
	0	USB Conn 1 (Power share)
	1	USB Conn 3 (Power share)
	2	USB Conn 2 (Power share)
	3	USB Conn 4 (Power share)
	4	JMINI1 (WLAN)
	5	None
	6	None
	7	None
	8	None
	9	Touch screen
	10	None
	11	None
	12	CAMERA
	13	None

USB3	DESTINATION
1	USB Conn 1 (Power share)
2	USB Conn 3 (Power share)
3	USB Conn 2 (Power share)
4	USB Conn 4 (Power share)

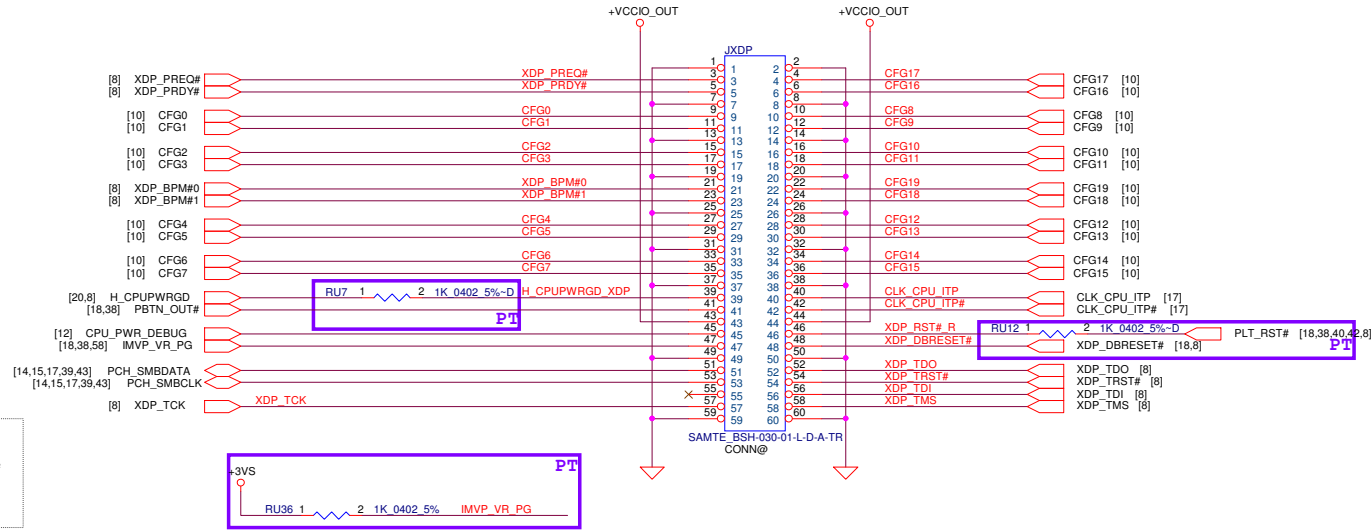
Symbol Note :



Security Classification	Compal Secret Data		Title	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Compal Electronics, Inc.
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RESEARCH AND DEVELOPMENT DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Notes List
Document Number				Rev
LA-7851P				0.1
Date: Tuesday, September 03, 2013				Sheet 4 of 62



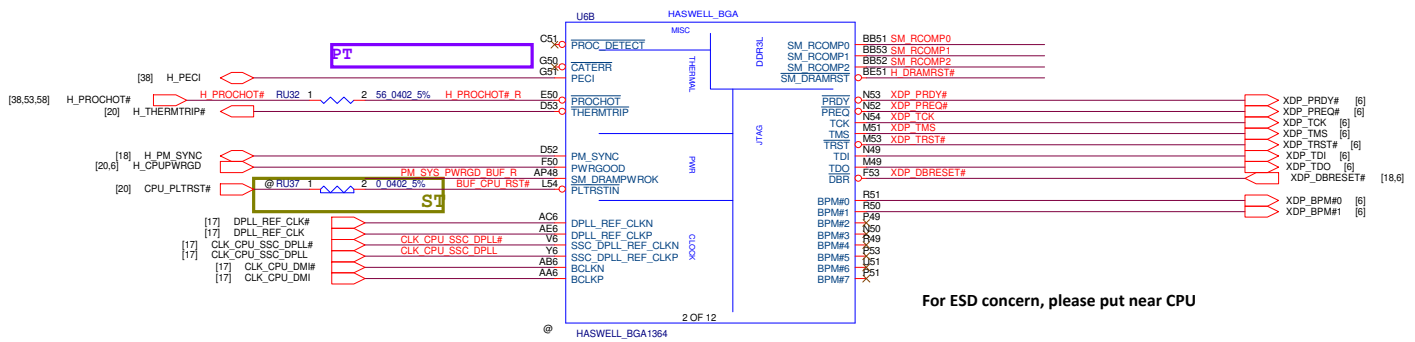
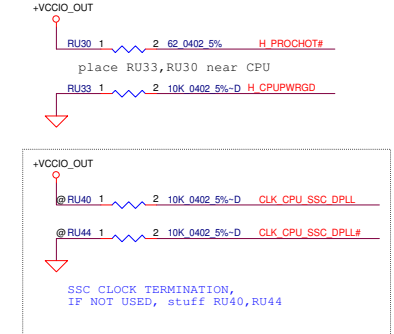
XDP CONN



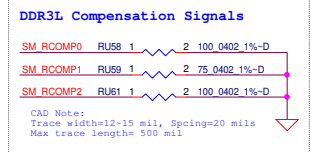
www.aitech1.ru

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	Block Diagram
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.1
				Date: Tuesday, September 03, 2013	Sheet 6 of 62

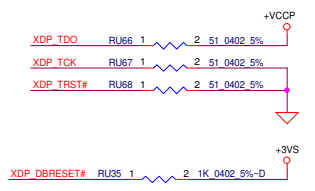
Processor Pullups



For ESD concern, please put near CPU

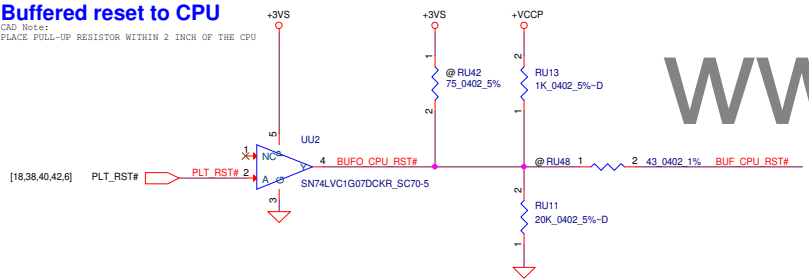


PU/PD for JTAG signals



Buffered reset to CPU

CAD Note:
PLACE PULL-UP RESISTOR WITHIN 2 INCH OF THE CPU

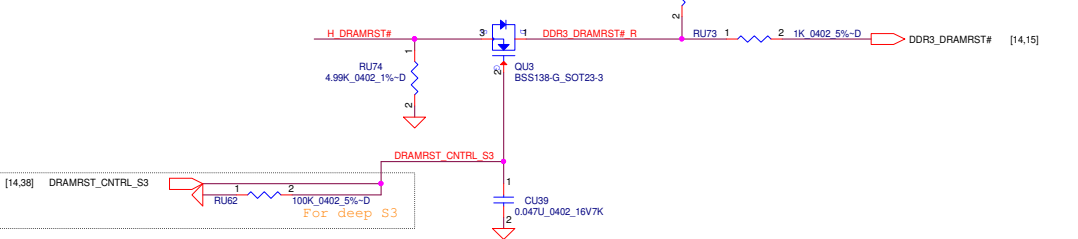
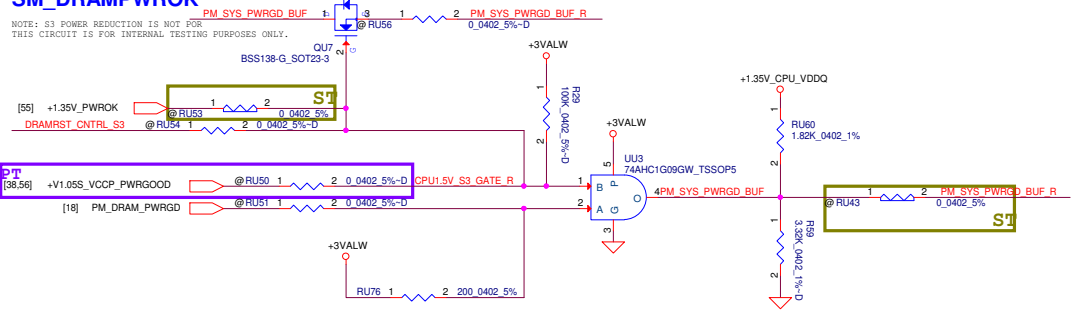


www.aitech1.ru

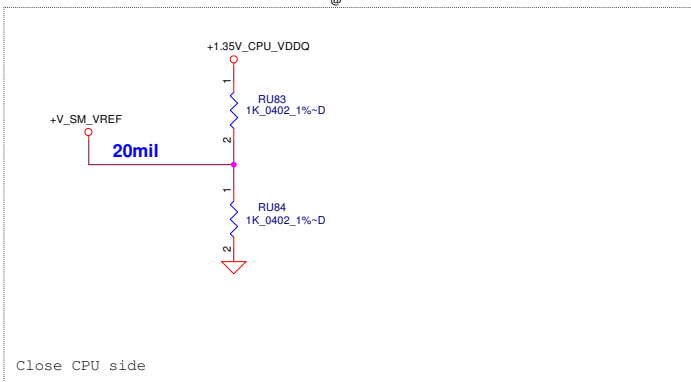
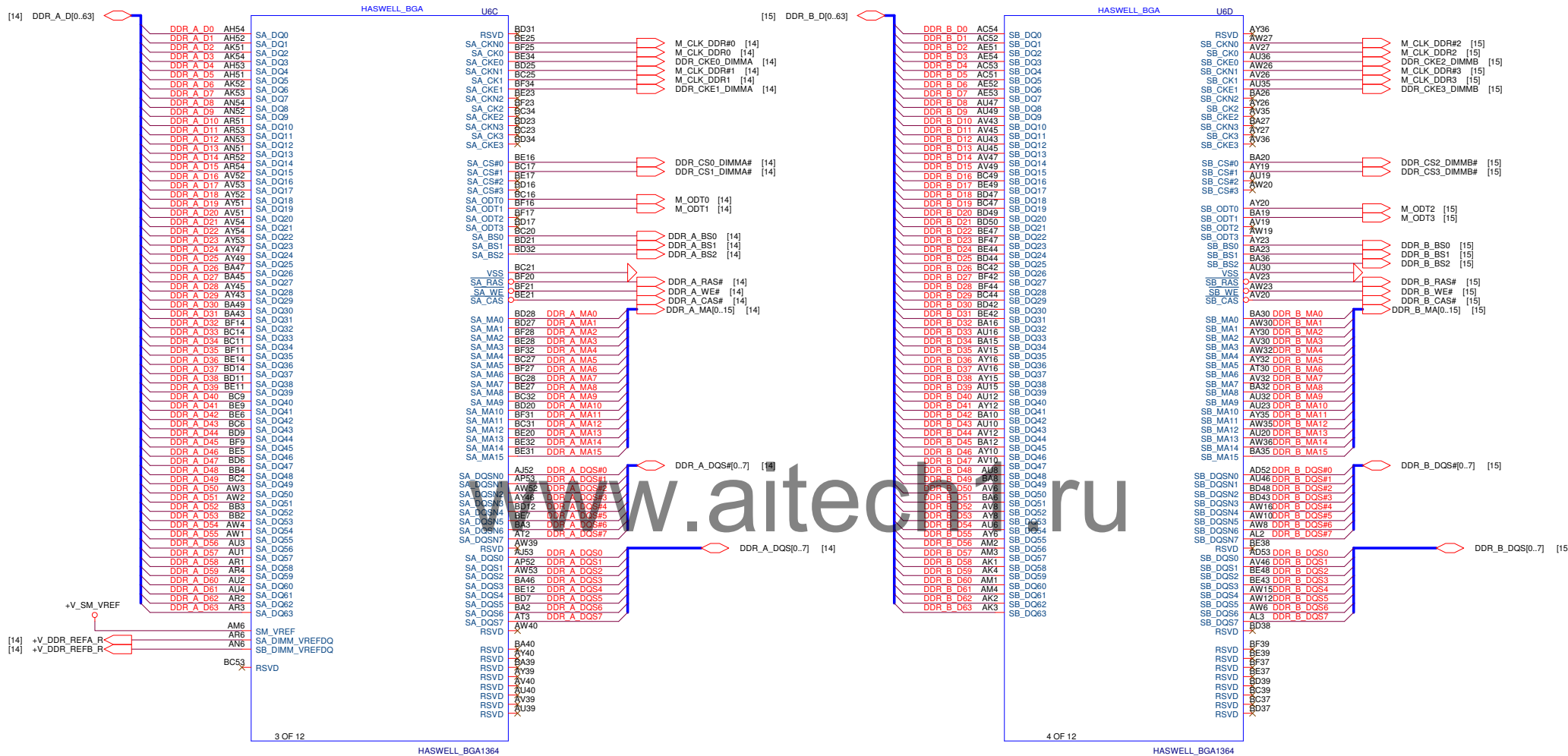
S3 circuit: DRAM_RST# to memory should be high during S3

SM_DRAMPWROK

NOTE: S3 POWER REDUCTION IS NOT FOR THIS CIRCUIT IS FOR INTERNAL TESTING PURPOSES ONLY.



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/08/25	Deciphered Date	2012/07/25
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			
Size	Custom	Document Number	PROCESSOR(2/7) PM,XDP,CLK
Date	Tuesday, September 03, 2013	Sheet	8 of 62

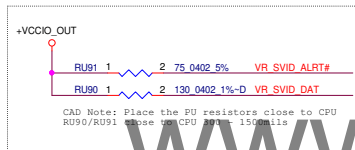
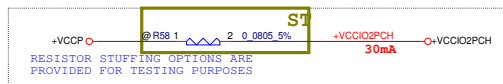
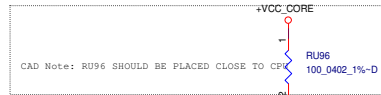
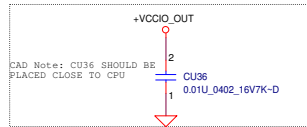
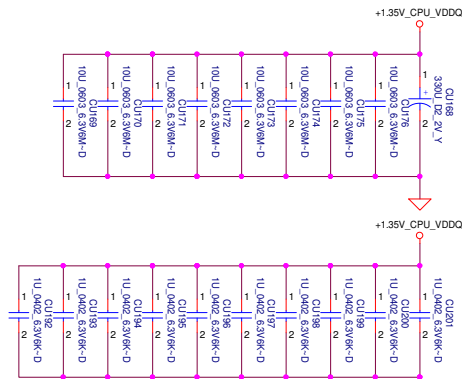
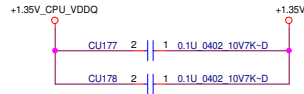


Security Classification		Compal Secret Data		Title	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Compal Electronics, Inc.	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.1
Date: Tuesday, September 03, 2013				Sheet 9	of 62

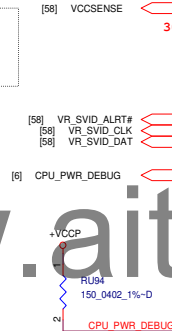
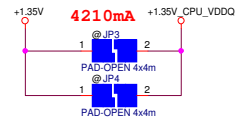
55A



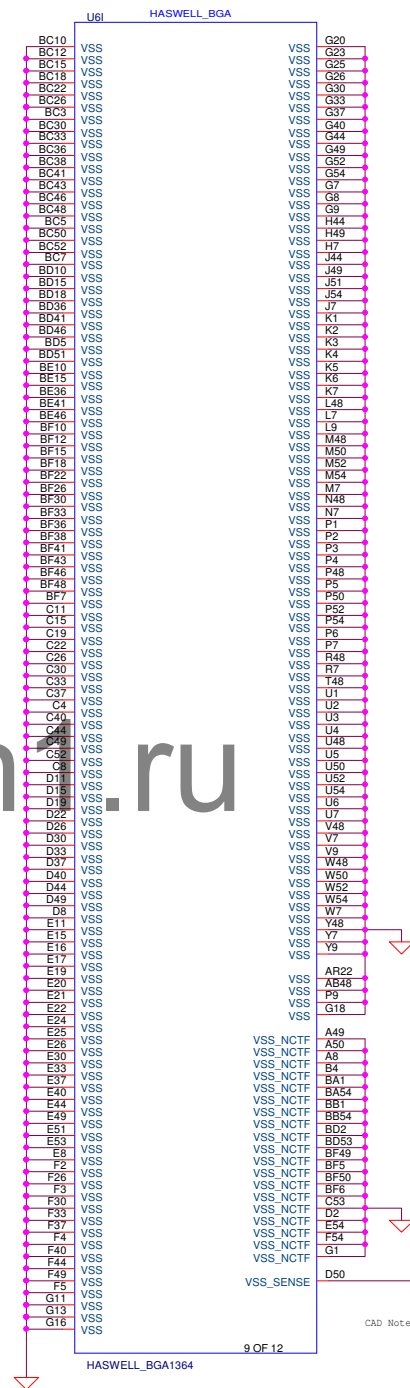
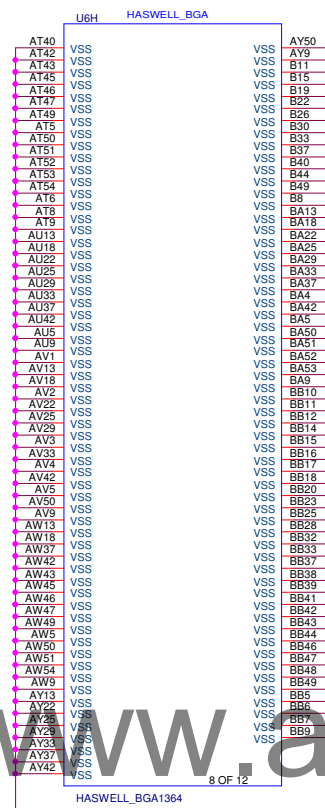
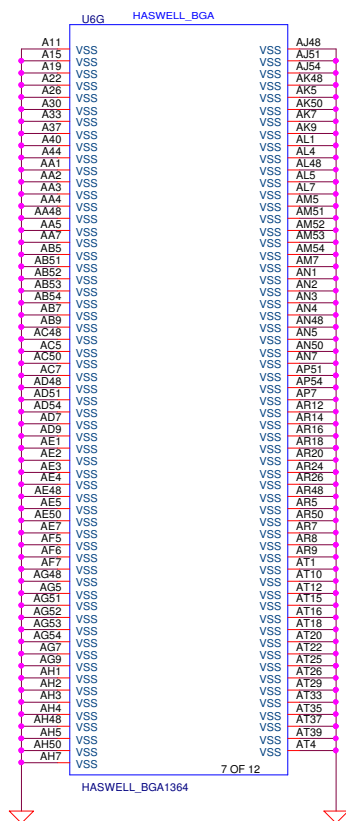
Security Classification		Compal Secret Data		Title	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Customer	PROCESSOR(5/7) PWR,BYPASS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev 0.1
Date: Tuesday, September 03, 2013				Sheet 11 of 62	



+1.35V_CPU_VDDQ Source



Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				PROCESSOR(6/7) PWR
Date: Tuesday, September 03, 2013		Sheet: 12 of 62		Rev: 0.1



Security Classification		Compal Secret Data		<i>Compal Electronics, Inc.</i> PROCESSOR(7/7) VSS	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF THE DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Rev	0.1
				Document Number	
Date:				Tuesday, September 03, 2013	Sheet 13 of 62

M1

[9] DDR_A_DQS#[0..7]

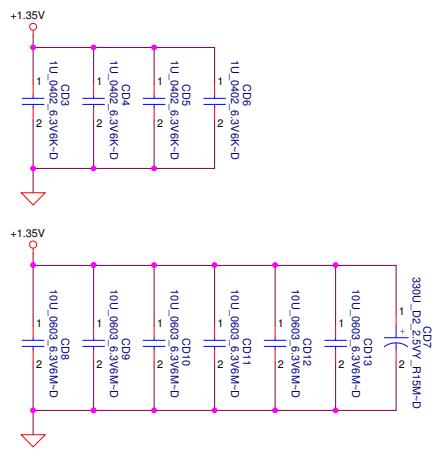
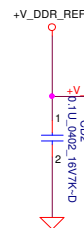
[9] DDR_A_DQS#[0..7]

[9] DDR_A_D[0..63]

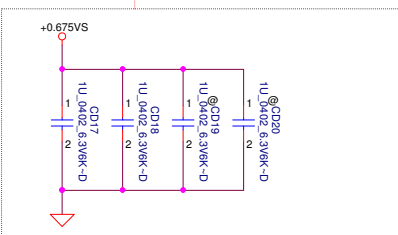
[9] DDR_A_MA[0..15]

All VREF traces should have 10 mil trace width

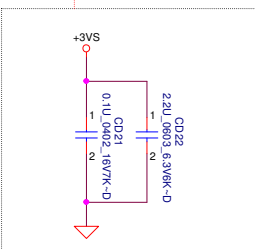
Layout Note:
Place near JDIMM1



Layout Note:
Place near JDIMM1.203,204



Layout Note:
Place near JDIMM1.199



[9] DDR_CKE0_DIMMA DDR_CKE0_DIMMA

[9] DDR_A_BS2 DDR_A_BS2

[9] M_CLK_DDR0 M_CLK_DDR#0

[9] DDR_A_BS0 DDR_A_BS0

[9] DDR_A_WE# DDR_A_WE#

[9] DDR_A_CAS# DDR_A_CAS#

[9] DDR_CS# DIMMA# DDR_CS# DIMMA#

[9] M_CLK_DDR1 M_CLK_DDR#1

[9] DDR_A_BS1 DDR_A_BS1

[9] DDR_CS0_DIMMA# DDR_CS0_DIMMA#

[9] M_ODT0 M_ODT0

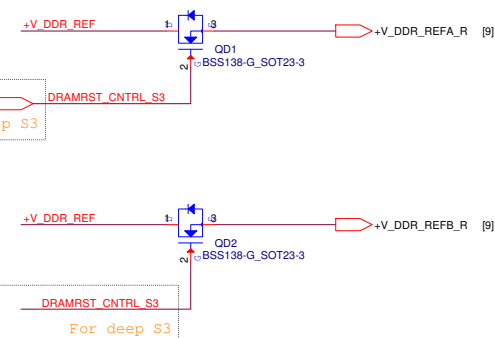
[9] M_ODT1 M_ODT1

All VREF traces should have 10 mil trace width

+V_DDR_REF

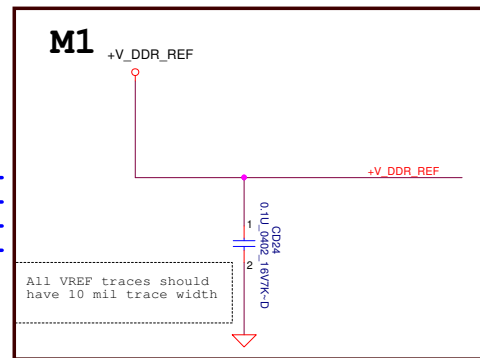


M3



M3 Circuit (Processor Generated SO-DIMM VREF_DQ)

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	
				DDRIII DIMMA	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev
				LA-7851P	0.1
				Date: Tuesday, September 03, 2013	Sheet 14 of 62



The diagram shows a parallel circuit with three branches connected to a $+0.675\text{V}$ source. Each branch contains a capacitor labeled with its value and type: $1\mu\text{F}0402, 5.39\text{V}K-C$. The capacitors are identified as CD42, CD44, and CD39. Each capacitor has a polarity marking with '1' on the positive terminal and '2' on the negative terminal. The negative terminals of all three capacitors are connected to a common ground point, indicated by a triangle symbol.

The diagram illustrates the electrical connection between a DDR3 DIMM and a PCB. The DIMM is shown on the left, with its pins connected to the PCB traces. The PCB traces are labeled with various signals, including address lines (A0-A15), data lines (D0-D31), and control signals (CS, RAS, CAS, WE, ODT, VREF, VSS, VDD, etc.). The DIMM is labeled with its pin numbers (1-28) and the corresponding signal names. The PCB is labeled with its pin numbers (1-28) and the corresponding signal names. The diagram also shows the connection of the DIMM to the PCB via a connector (CONN@).

Signal Connections:

- Address Lines:** A0-A15 (DIMM pins 1-16) to PCB pins 1-16.
- Data Lines:** D0-D31 (DIMM pins 17-48) to PCB pins 17-48.
- Control Signals:** CS, RAS, CAS, WE, ODT, VREF, VSS, VDD, etc. (DIMM pins 49-100) to PCB pins 49-100.
- Power/Ground:** VDD, VSS, GND, BOSS1, BOSS2, BOSS3, BOSS4, BOSS5, BOSS6, BOSS7, BOSS8, BOSS9, BOSS10, BOSS11, BOSS12, BOSS13, BOSS14, BOSS15, BOSS16, BOSS17, BOSS18, BOSS19, BOSS20, BOSS21, BOSS22, BOSS23, BOSS24, BOSS25, BOSS26, BOSS27, BOSS28, BOSS29, BOSS30, BOSS31, BOSS32, BOSS33, BOSS34, BOSS35, BOSS36, BOSS37, BOSS38, BOSS39, BOSS40, BOSS41, BOSS42, BOSS43, BOSS44, BOSS45, BOSS46, BOSS47, BOSS48, BOSS49, BOSS50, BOSS51, BOSS52, BOSS53, BOSS54, BOSS55, BOSS56, BOSS57, BOSS58, BOSS59, BOSS60, BOSS61, BOSS62, BOSS63, BOSS64, BOSS65, BOSS66, BOSS67, BOSS68, BOSS69, BOSS70, BOSS71, BOSS72, BOSS73, BOSS74, BOSS75, BOSS76, BOSS77, BOSS78, BOSS79, BOSS80, BOSS81, BOSS82, BOSS83, BOSS84, BOSS85, BOSS86, BOSS87, BOSS88, BOSS89, BOSS90, BOSS91, BOSS92, BOSS93, BOSS94, BOSS95, BOSS96, BOSS97, BOSS98, BOSS99, BOSS100.

Component Labels:

- DDR3 DIMM:** DDR3 DIMM, DDR3 DIMM#1, DDR3 DIMM#2, DDR3 DIMM#3, DDR3 DIMM#4, DDR3 DIMM#5, DDR3 DIMM#6, DDR3 DIMM#7, DDR3 DIMM#8, DDR3 DIMM#9, DDR3 DIMM#10, DDR3 DIMM#11, DDR3 DIMM#12, DDR3 DIMM#13, DDR3 DIMM#14, DDR3 DIMM#15, DDR3 DIMM#16, DDR3 DIMM#17, DDR3 DIMM#18, DDR3 DIMM#19, DDR3 DIMM#20, DDR3 DIMM#21, DDR3 DIMM#22, DDR3 DIMM#23, DDR3 DIMM#24, DDR3 DIMM#25, DDR3 DIMM#26, DDR3 DIMM#27, DDR3 DIMM#28, DDR3 DIMM#29, DDR3 DIMM#30, DDR3 DIMM#31, DDR3 DIMM#32, DDR3 DIMM#33, DDR3 DIMM#34, DDR3 DIMM#35, DDR3 DIMM#36, DDR3 DIMM#37, DDR3 DIMM#38, DDR3 DIMM#39, DDR3 DIMM#40, DDR3 DIMM#41, DDR3 DIMM#42, DDR3 DIMM#43, DDR3 DIMM#44, DDR3 DIMM#45, DDR3 DIMM#46, DDR3 DIMM#47, DDR3 DIMM#48, DDR3 DIMM#49, DDR3 DIMM#50, DDR3 DIMM#51, DDR3 DIMM#52, DDR3 DIMM#53, DDR3 DIMM#54, DDR3 DIMM#55, DDR3 DIMM#56, DDR3 DIMM#57, DDR3 DIMM#58, DDR3 DIMM#59, DDR3 DIMM#60, DDR3 DIMM#61, DDR3 DIMM#62, DDR3 DIMM#63, DDR3 DIMM#64, DDR3 DIMM#65, DDR3 DIMM#66, DDR3 DIMM#67, DDR3 DIMM#68, DDR3 DIMM#69, DDR3 DIMM#70, DDR3 DIMM#71, DDR3 DIMM#72, DDR3 DIMM#73, DDR3 DIMM#74, DDR3 DIMM#75, DDR3 DIMM#76, DDR3 DIMM#77, DDR3 DIMM#78, DDR3 DIMM#79, DDR3 DIMM#80, DDR3 DIMM#81, DDR3 DIMM#82, DDR3 DIMM#83, DDR3 DIMM#84, DDR3 DIMM#85, DDR3 DIMM#86, DDR3 DIMM#87, DDR3 DIMM#88, DDR3 DIMM#89, DDR3 DIMM#90, DDR3 DIMM#91, DDR3 DIMM#92, DDR3 DIMM#93, DDR3 DIMM#94, DDR3 DIMM#95, DDR3 DIMM#96, DDR3 DIMM#97, DDR3 DIMM#98, DDR3 DIMM#99, DDR3 DIMM#100.
- PCB:** PCB, PCB#1, PCB#2, PCB#3, PCB#4, PCB#5, PCB#6, PCB#7, PCB#8, PCB#9, PCB#10, PCB#11, PCB#12, PCB#13, PCB#14, PCB#15, PCB#16, PCB#17, PCB#18, PCB#19, PCB#20, PCB#21, PCB#22, PCB#23, PCB#24, PCB#25, PCB#26, PCB#27, PCB#28, PCB#29, PCB#30, PCB#31, PCB#32, PCB#33, PCB#34, PCB#35, PCB#36, PCB#37, PCB#38, PCB#39, PCB#40, PCB#41, PCB#42, PCB#43, PCB#44, PCB#45, PCB#46, PCB#47, PCB#48, PCB#49, PCB#50, PCB#51, PCB#52, PCB#53, PCB#54, PCB#55, PCB#56, PCB#57, PCB#58, PCB#59, PCB#60, PCB#61, PCB#62, PCB#63, PCB#64, PCB#65, PCB#66, PCB#67, PCB#68, PCB#69, PCB#70, PCB#71, PCB#72, PCB#73, PCB#74, PCB#75, PCB#76, PCB#77, PCB#78, PCB#79, PCB#80, PCB#81, PCB#82, PCB#83, PCB#84, PCB#85, PCB#86, PCB#87, PCB#88, PCB#89, PCB#90, PCB#91, PCB#92, PCB#93, PCB#94, PCB#95, PCB#96, PCB#97, PCB#98, PCB#99, PCB#100.

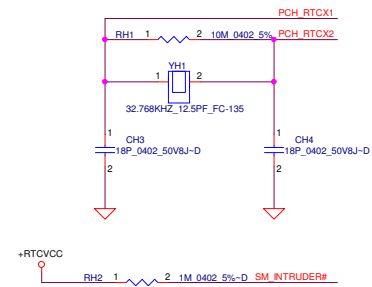
Other Labels:

- CONN@:** Connector label.
- 0.1U 0402 16V-K-D:** Component value.
- BELLW_80001-1021:** Component part number.

0.1uF 0402 16V7K-D

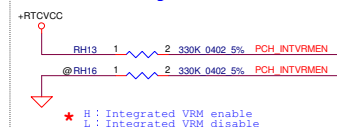
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	DDRIII DIMMB LA-7851P
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	
Date: Tuesday, September 03, 2013				Sheet	15 of 62

RTC CRYSTAL

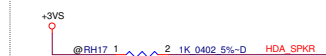


PCH Strap PIN

INTVRMEN Integrated 1.05V VRM Enable/Disable

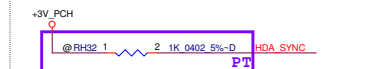


SPKR No Reboot

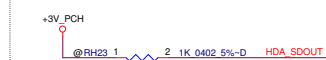


If the signal is sampled high, this indicate that the system is strapped to the "No Reboot" mode

HDA_SYNC On-Die PLL Voltage Regulator Voltage Select

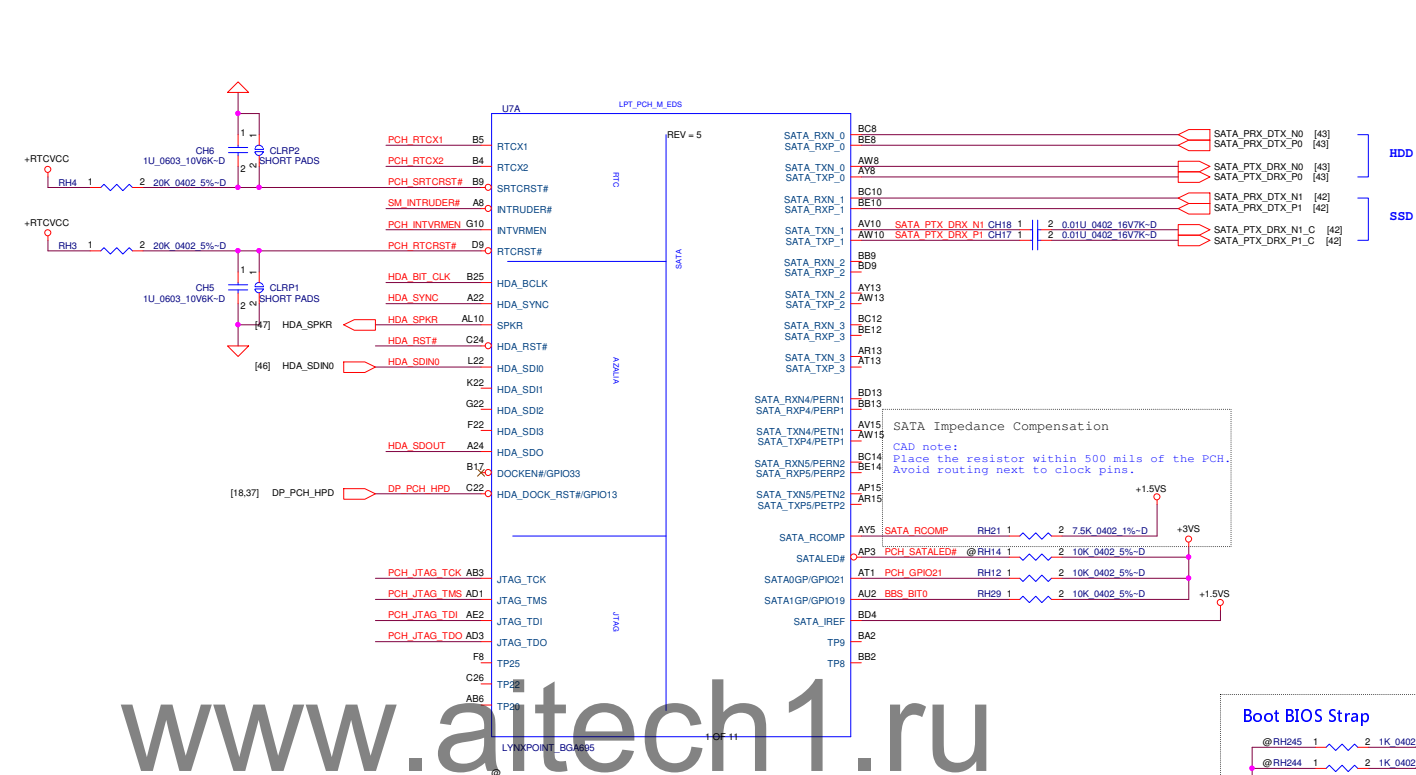
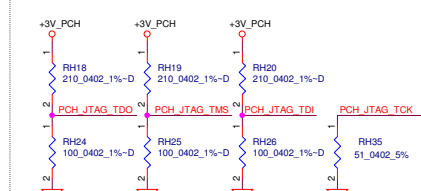


HDA_SDO Flash Descriptor Security Override/Intel ME Debug Mode

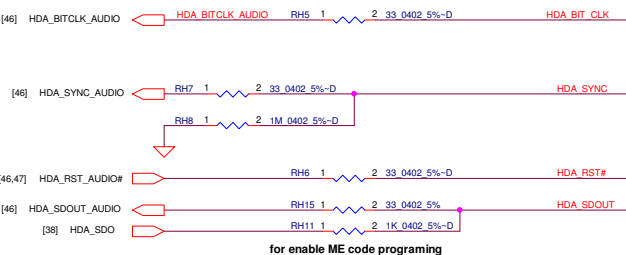


ME debug mode, this signal has a weak internal PD
L=>security measures defined in the Flash Descriptor will be in effect (default)
H=>Flash Descriptor Security will be overridden

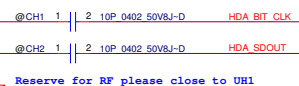
JTAG



HD Audio



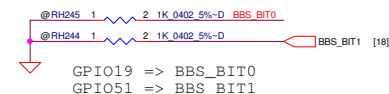
Reserve for EMI



RTC Battery

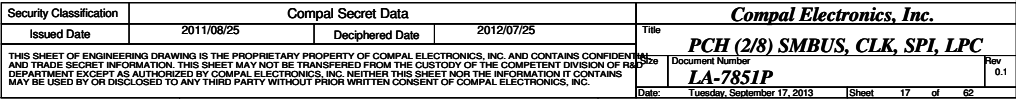


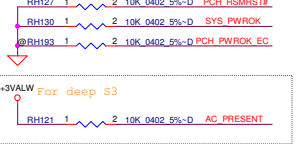
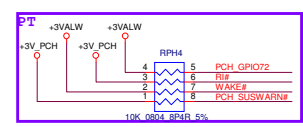
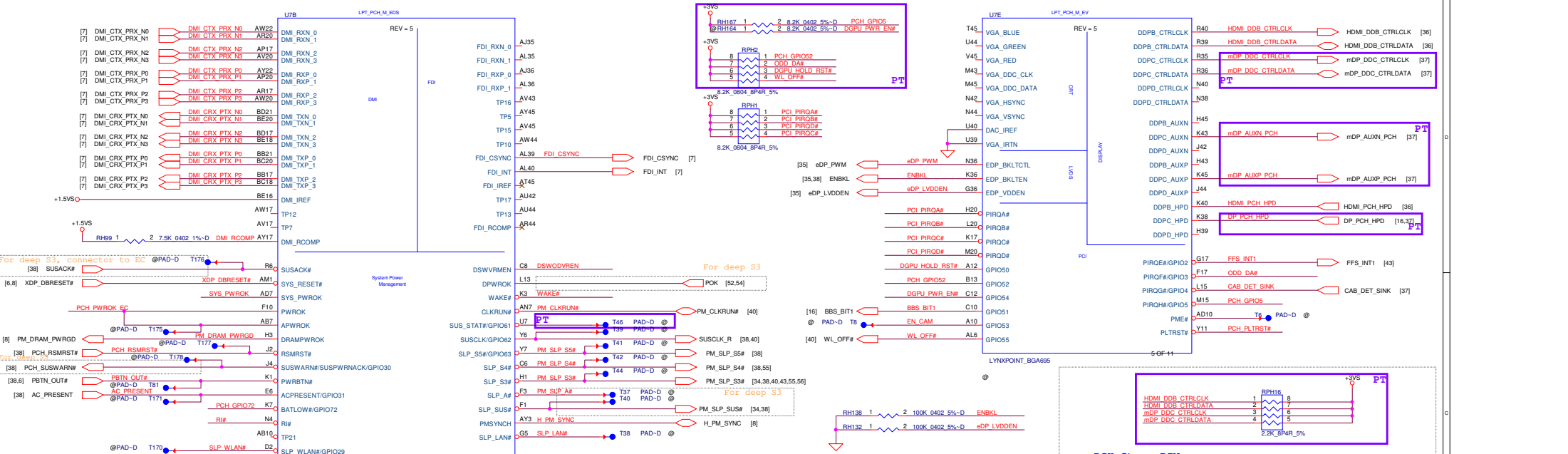
Boot BIOS Strap



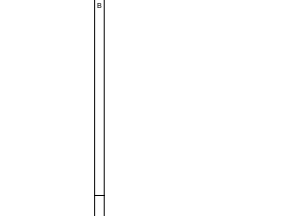
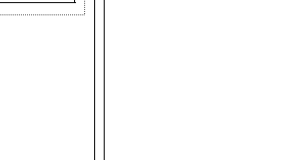
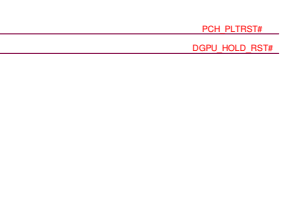
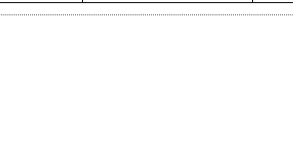
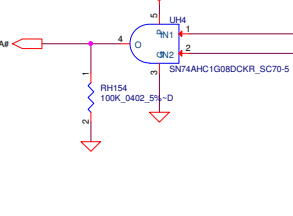
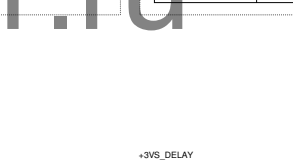
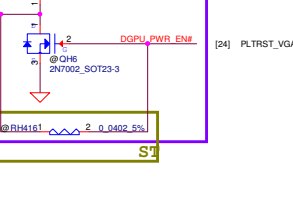
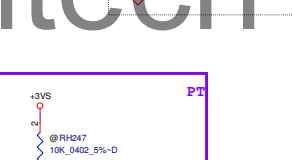
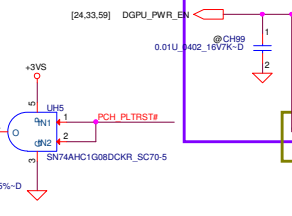
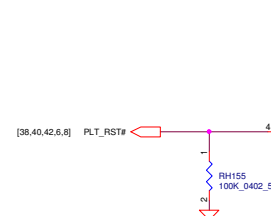
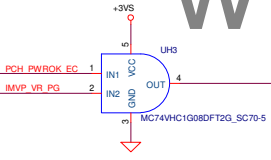
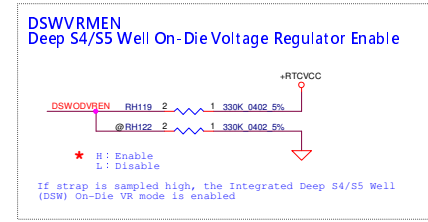
Boot BIOS Strap

BBS_BIT[1]	BBS_BIT[0]	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI





PCH Strap PIN

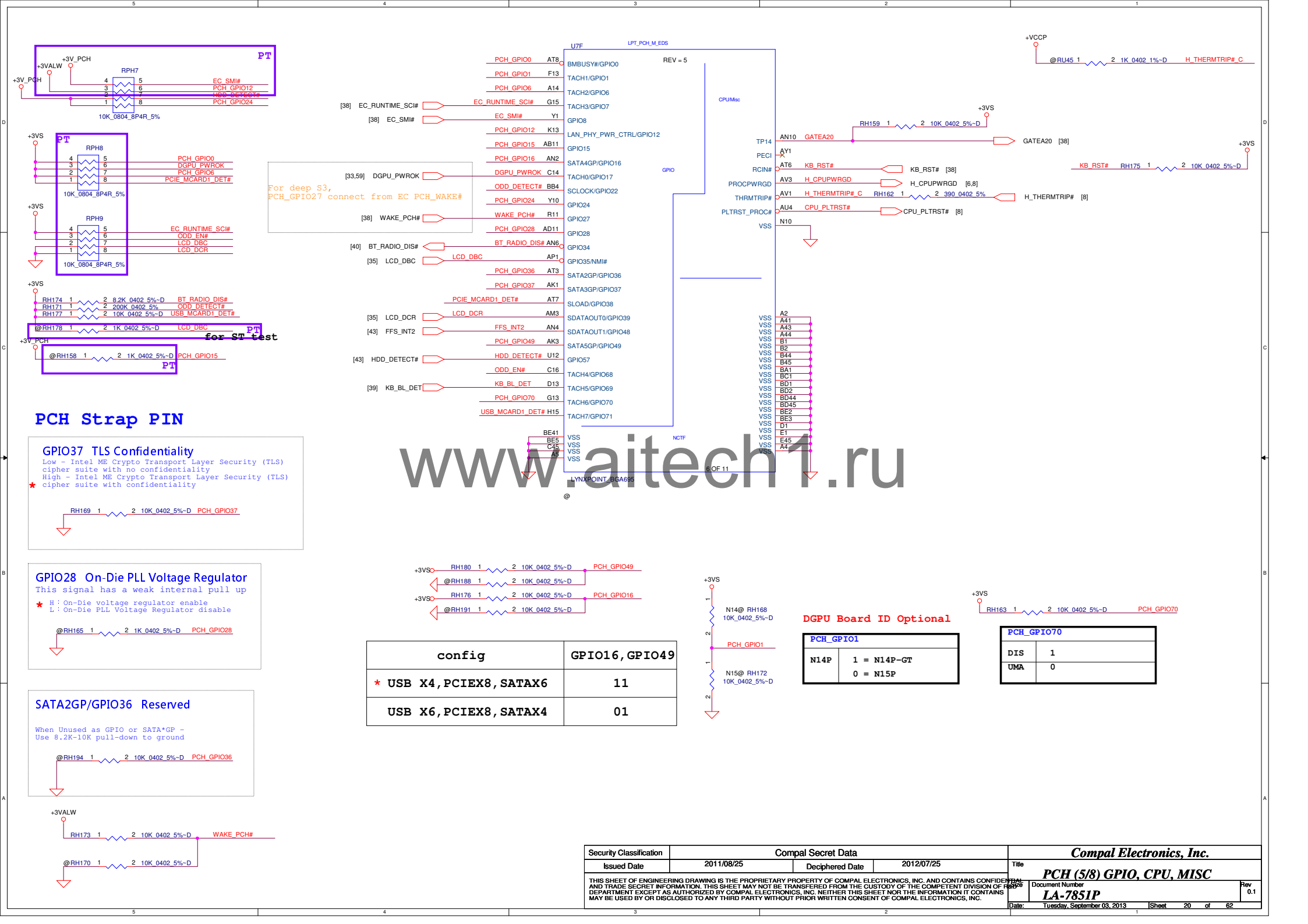


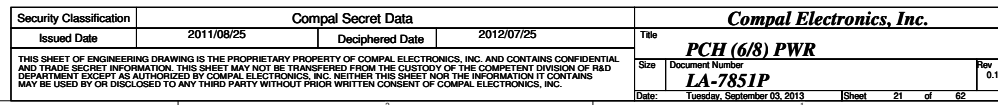
PCH Strap PIN

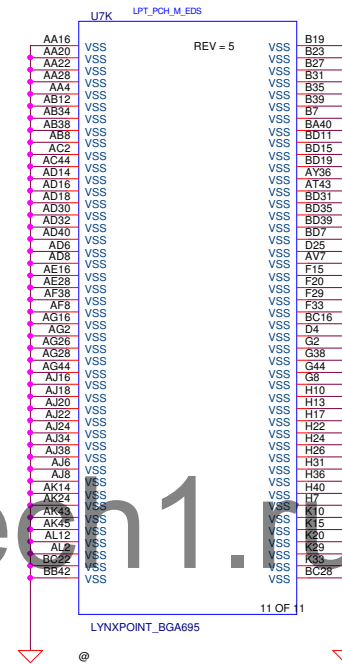
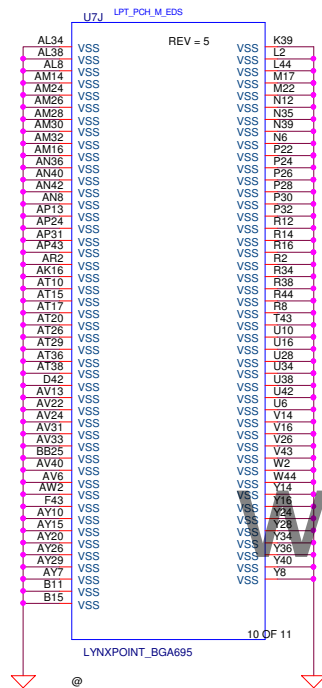
DisplayPort* Disabling and Termination Guidelines

Port	Strap	How to Enable Port?	How to Disable Port?
Port B	DDPB_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω \pm 5% resistor	No Connect
Port C	DDPC_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω \pm 5% resistor	No Connect
Port D	DDPD_CTRLDATA	Pull up to 3.3 V with 2.2-k Ω \pm 5% resistor	No Connect

www.aitech1.ru







Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	PCH (8/8) VSS
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF HARP DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-7851P
				Date: Tuesday, September 03, 2013	Rev 0.1
				Sheet 23 of 62	

[7] PEG_HTX_C_GRX_P[0..15] PEG_HTX_C_GRX_P[0..15]
 [7] PEG_HTX_C_GRX_N[0..15] PEG_HTX_C_GRX_N[0..15]
 [7] PEG_GTX_C_HRX_P[0..15] PEG_GTX_C_HRX_P[0..15]
 [7] PEG_GTX_C_HRX_N[0..15] PEG_GTX_C_HRX_N[0..15]

PEG GTX C_HRX_P0	CV531	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P0
PEG GTX C_HRX_N0	CV532	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N0
PEG GTX C_HRX_P1	CV533	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P1
PEG GTX C_HRX_N1	CV534	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N1
PEG GTX C_HRX_P2	CV535	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P2
PEG GTX C_HRX_N2	CV536	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N2
PEG GTX C_HRX_P3	CV537	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P3
PEG GTX C_HRX_N3	CV538	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N3
PEG GTX C_HRX_P4	CV539	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P4
PEG GTX C_HRX_N4	CV540	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N4
PEG GTX C_HRX_P5	CV541	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P5
PEG GTX C_HRX_N5	CV542	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N5
PEG GTX C_HRX_P6	CV543	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P6
PEG GTX C_HRX_N6	CV544	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N6
PEG GTX C_HRX_P7	CV545	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P7
PEG GTX C_HRX_N7	CV546	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N7
PEG GTX C_HRX_P8	CV547	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P8
PEG GTX C_HRX_N8	CV548	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N8
PEG GTX C_HRX_P9	CV550	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P9
PEG GTX C_HRX_N9	CV551	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N9
PEG GTX C_HRX_P10	CV552	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P10
PEG GTX C_HRX_N10	CV553	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N10
PEG GTX C_HRX_P11	CV558	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P11
PEG GTX C_HRX_N11	CV559	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N11
PEG GTX C_HRX_P12	CV560	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P12
PEG GTX C_HRX_N12	CV561	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N12
PEG GTX C_HRX_P13	CV562	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P13
PEG GTX C_HRX_N13	CV563	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N13
PEG GTX C_HRX_P14	CV564	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P14
PEG GTX C_HRX_N14	CV565	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N14
PEG GTX C_HRX_P15	CV566	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_P15
PEG GTX C_HRX_N15	CV567	2	1	0.22U	0402	16V7K-D	PEG GTX HRX_N15

[17] CLK_PEG_VGA# PEX_TSTCLK_OUT#
 [17] CLK_PEG_VGA# PEX_TSTCLK_OUT#
 [18] PLTRST_VGA# PEX_TSTCLK_OUT#
 [17] PEG_A_CLKRQ# CLK_REQ#

PEG_HTX_C_GRX_P0 AN12
 PEG_HTX_C_GRX_N0 AN12
 PEG_HTX_C_GRX_P1 AN14
 PEG_HTX_C_GRX_N1 AN14
 PEG_HTX_C_GRX_P2 AP14
 PEG_HTX_C_GRX_N2 AP14
 PEG_HTX_C_GRX_P3 AN15
 PEG_HTX_C_GRX_N3 AN15
 PEG_HTX_C_GRX_P4 AN17
 PEG_HTX_C_GRX_N4 AN17
 PEG_HTX_C_GRX_P5 AP17
 PEG_HTX_C_GRX_N5 AP17
 PEG_HTX_C_GRX_P6 AN18
 PEG_HTX_C_GRX_N6 AN18
 PEG_HTX_C_GRX_P7 AN20
 PEG_HTX_C_GRX_N7 AN20
 PEG_HTX_C_GRX_P8 AP20
 PEG_HTX_C_GRX_N8 AP20
 PEG_HTX_C_GRX_P9 AN21
 PEG_HTX_C_GRX_N9 AN21
 PEG_HTX_C_GRX_P10 AN23
 PEG_HTX_C_GRX_N10 AN23
 PEG_HTX_C_GRX_P11 AP23
 PEG_HTX_C_GRX_N11 AP23
 PEG_HTX_C_GRX_P12 AN24
 PEG_HTX_C_GRX_N12 AN24
 PEG_HTX_C_GRX_P13 AN26
 PEG_HTX_C_GRX_N13 AN26
 PEG_HTX_C_GRX_P14 AP26
 PEG_HTX_C_GRX_N14 AP26
 PEG_HTX_C_GRX_P15 AN27
 PEG_HTX_C_GRX_N15 AN27

PEG GTX HRX_P0 AK14
 PEG GTX HRX_N0 AJ14
 PEG GTX HRX_P1 AH14
 PEG GTX HRX_N1 AG14
 PEG GTX HRX_P2 AK15
 PEG GTX HRX_N2 AJ15
 PEG GTX HRX_P3 AL16
 PEG GTX HRX_N3 AK16
 PEG GTX HRX_P4 AK17
 PEG GTX HRX_N4 AJ17
 PEG GTX HRX_P5 AH17
 PEG GTX HRX_N5 AG17
 PEG GTX HRX_P6 AK18
 PEG GTX HRX_N6 AJ18
 PEG GTX HRX_P7 AL19
 PEG GTX HRX_N7 AK19
 PEG GTX HRX_P8 AK20
 PEG GTX HRX_N8 AJ20
 PEG GTX HRX_P9 AH20
 PEG GTX HRX_N9 AG20
 PEG GTX HRX_P10 AK21
 PEG GTX HRX_N10 AJ21
 PEG GTX HRX_P11 AL22
 PEG GTX HRX_N11 AK22
 PEG GTX HRX_P12 AK23
 PEG GTX HRX_N12 AJ23
 PEG GTX HRX_P13 AH23
 PEG GTX HRX_N13 AG23
 PEG GTX HRX_P14 AK24
 PEG GTX HRX_N14 AJ24
 PEG GTX HRX_P15 AL25
 PEG GTX HRX_N15 AK25

Part 1 of 7

GPIO

DACS

I2C

CLK

GPIO0
 GPIO1
 GPIO2
 GPIO3
 GPIO4
 GPIO5
 GPIO6
 GPIO7
 GPIO8
 GPIO9
 GPIO10
 GPIO11
 GPIO12
 GPIO13
 GPIO14
 GPIO15
 GPIO16
 GPIO17
 GPIO18
 GPIO19
 GPIO20
 GPIO21

DACA_RED
 DACA_GREEN
 DACA_BLUE
 DACA_HSYNC
 DACA_VSYNC
 DACA_VDD
 DACA_VREF
 DACA_RSET

I2CA_SCL
 I2CA_SDA
 I2CB_SCL
 I2CB_SDA
 I2CC_SCL
 I2CC_SDA

PLLVD
 SP_PLLVD
 VID_PLLVD
 XTAL_IN
 XTAL_OUT
 XTAL_SSIN
 XTAL_OUTBUFF

PEX_REFCLK
 PEX_REFCLK_N
 PEX_CLKREQ_N
 PEX_TSTCLK_OUT
 PEX_TSTCLK_OUT_N
 PEX_RST_N
 PEX_TERM

FB_CLAMP_MON_R
 GPU_GPIO2
 GPU_GPIO3
 GPU_GPIO4
 FB_CLAMP_REQ#_Q
 GPU_GPIO7
 THM_OVERT#_R
 THM_ALERT#
 FBVREF_ALTV
 GPU_VID_0
 GPU_HOT#_R
 GPU_HOT#_R
 GPU_GPIO13

GPU_HOT#_R
 GPU_HOT#_R
 FB_CLAMP_REQ#_Q
 GPU_HOT#_R
 GPU_HOT#_R
 GPU_HOT#_R

THM_OVERT#_R
 THM_OVERT#_R
 THM_OVERT#_R
 THM_OVERT#_R
 THM_OVERT#_R
 THM_OVERT#_R

EC_SMB_CLK2_PX
 EC_SMB_CLK2_PX
 EC_SMB_CLK2_PX
 EC_SMB_CLK2_PX
 EC_SMB_CLK2_PX
 EC_SMB_CLK2_PX

CV773
 CV773
 CV773
 CV773
 CV773
 CV773

CV773
 CV773
 CV773
 CV773
 CV773
 CV773

CV773
 CV773
 CV773
 CV773
 CV773
 CV773

CV773
 CV773
 CV773
 CV773
 CV773
 CV773

CV773
 CV773
 CV773
 CV773
 CV773
 CV773

CV773
 CV773
 CV773
 CV773
 CV773
 CV773

RPH12
 GPU_GPIO2
 GPU_GPIO3
 GPU_GPIO4
 GPU_GPIO7

RPH33
 GPU_HOT#_R
 THM_OVERT#_R
 THM_ALERT#
 FBVREF_ALTV

RPH32
 CLK_REQ#
 FB_CLAMP_REQ#_Q
 XTALSSIN
 XTALOUTBUFF

RPH15
 I2CA_SCL
 I2CA_SDA
 I2CB_SCL
 I2CB_SDA

RPH13
 I2CC_SCL
 I2CC_SDA
 I2CC_SCL
 I2CC_SDA

BLM18PG300SN1D_2P
 BLM18PG300SN1D_2P
 BLM18PG300SN1D_2P
 BLM18PG300SN1D_2P

BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D

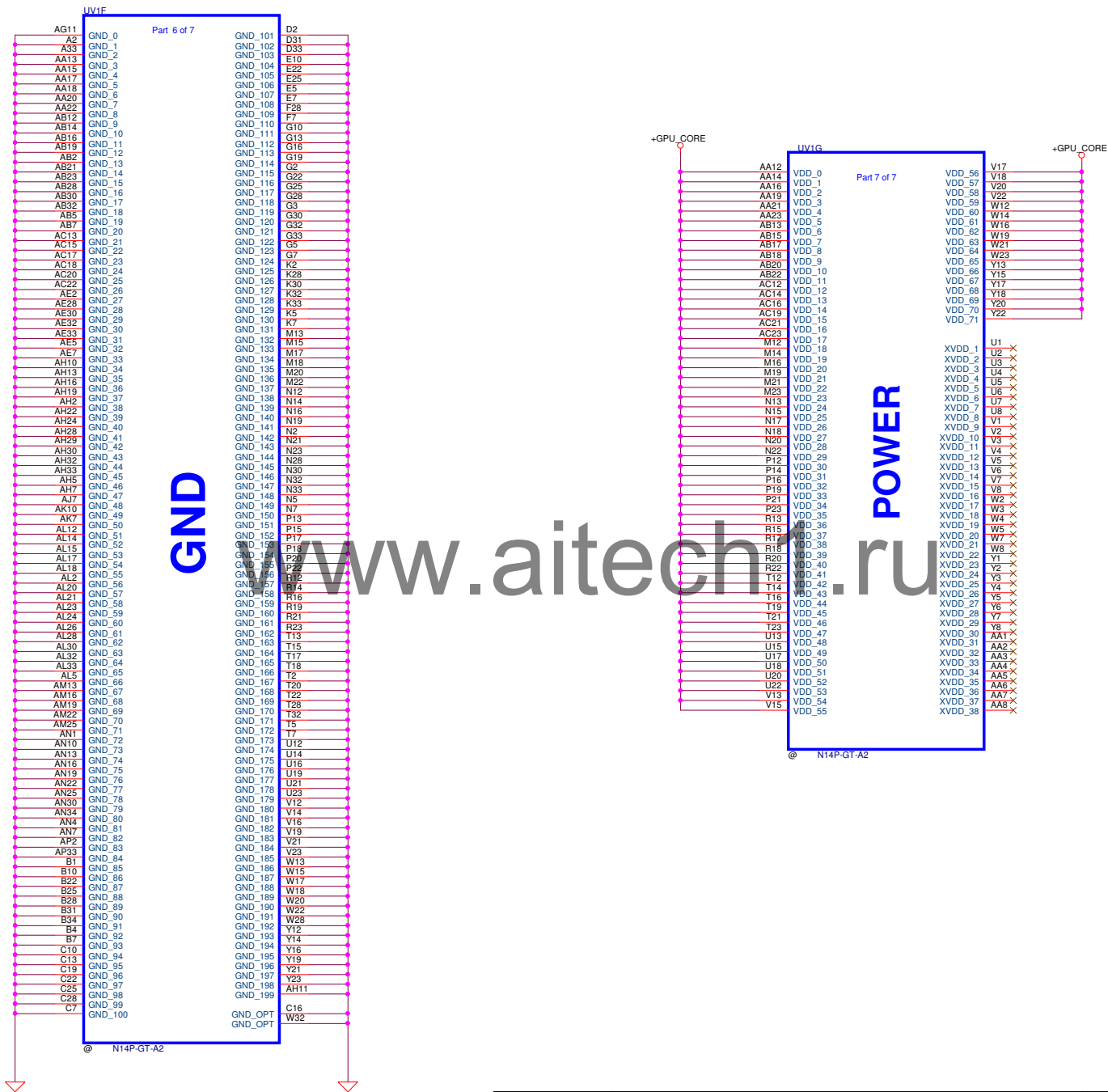
BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D

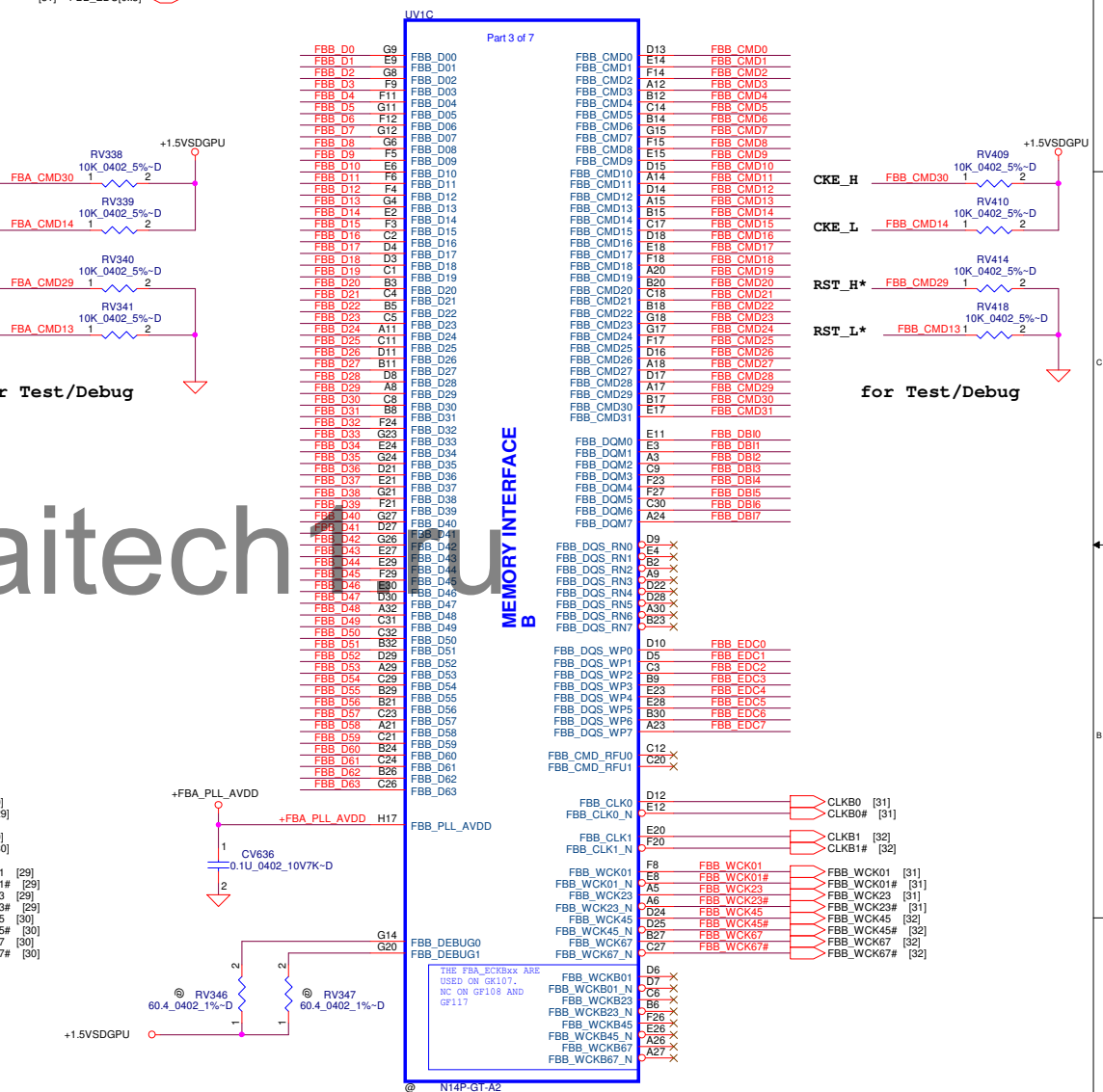
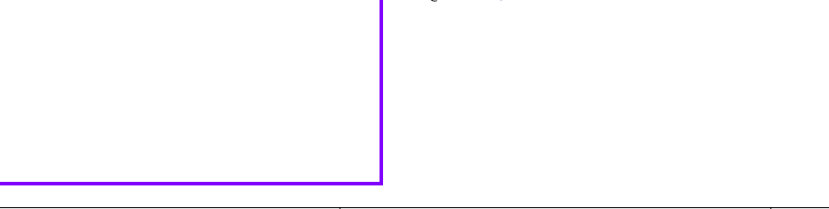
BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D

BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D

BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D
 BLM18PG181SN1_0603-D

Security Classification	Compal Secret Data	Document Number	Rev
Issued Date	2011/08/25	Deciphered Date	2012/07/25
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			
Date: Tuesday, September 03, 2013			Sheet 24 of 62





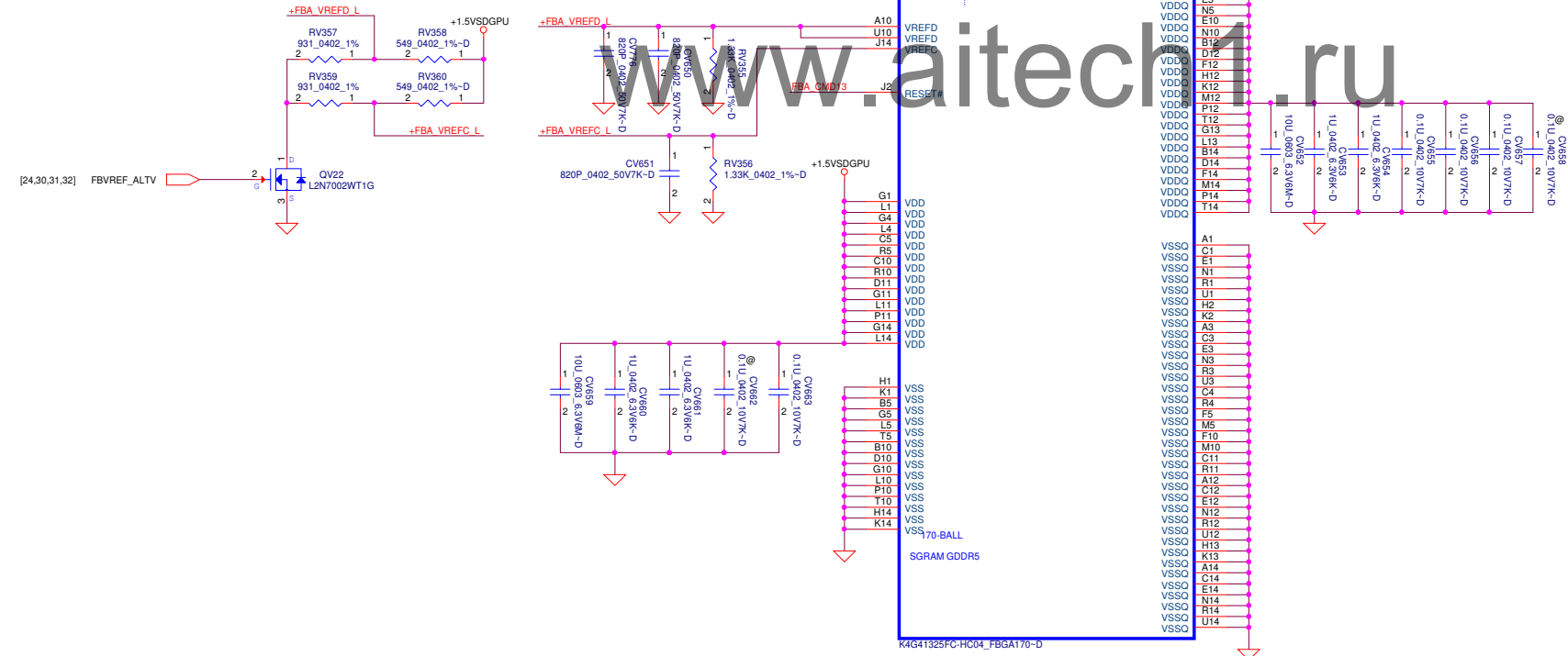
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	Block Diagram	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FORD MOTOR CREDIT TO ANY OTHER DEPARTMENT AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Doc No	Document Number	Rev 0.1
				Date:	Tuesday, September 03, 2013	Sheet 26 of 62

Memory Partition A - Lower 32 bits

64X32 GDDR5

Table 46. GDDR5 Mode H Mapping

GB2-64, GB4-128	Channel 0 0...31	GB2-64, GB4-128	Channel 1 32...63
CMD0	C5*	CMD16	C5*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RAS*	CMD28	RAS*
CMD13	RST*	CMD29	RST*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*



64X32 GDDR5

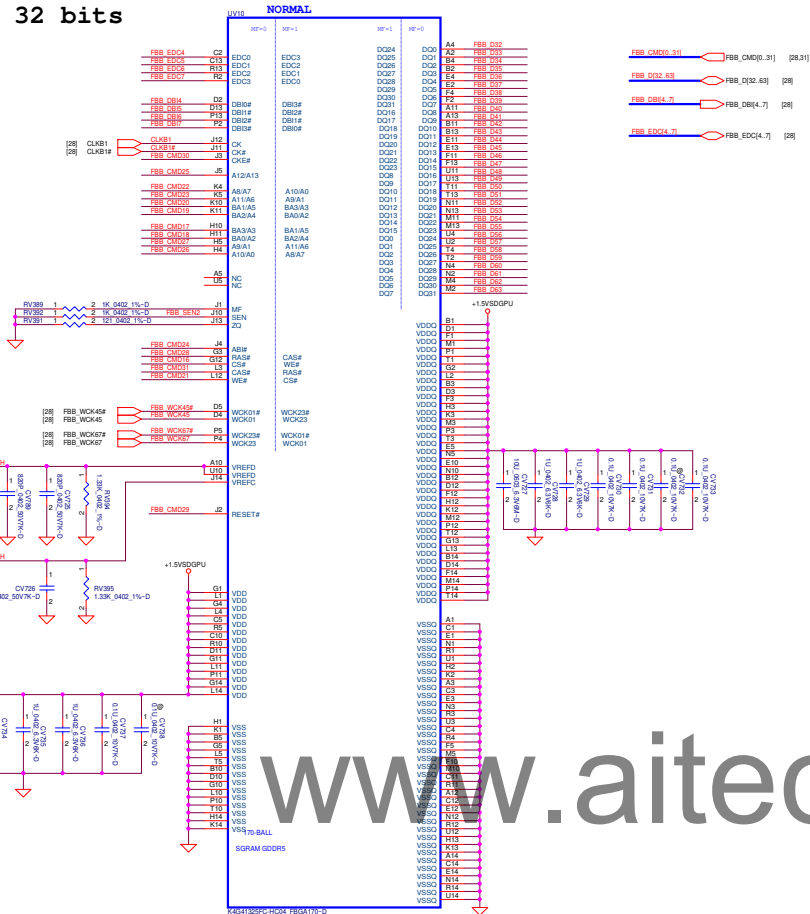
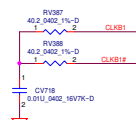
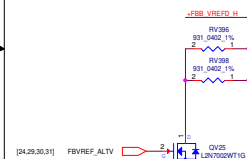
GB2-64, GB4-128	Channel 0 0..31	GB2-64, GB4-128	Channel 1 32..63
CMD0	CS*	CMD16	CS*
CMD1	A3_BA3	CMD17	A3_BA3
CMD2	A2_BA0	CMD18	A2_BA0
CMD3	A4_BA2	CMD19	A4_BA2
CMD4	A5_BA1	CMD20	A5_BA1
CMD5	WE*	CMD21	WE*
CMD6	A7_A8	CMD22	A7_A8
CMD7	A6_A11	CMD23	A6_A11
CMD8	AB1*	CMD24	AB1*
CMD9	A12_RFU	CMD25	A12_RFU
CMD10	A0_A10	CMD26	A0_A10
CMD11	A1_A9	CMD27	A1_A9
CMD12	RA5*	CMD28	RA5*
CMD13	R5T*	CMD29	R5T*
CMD14	CKE*	CMD30	CKE*
CMD15	CAS*	CMD31	CAS*

Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	Block Diagram	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FIRST DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number		
				Date:	Tuesday, September 03, 2013	Sheet 31 of 62

Memory Partition B - Upper 32 bits

Table 46. GDDR5 Mode H Mapping

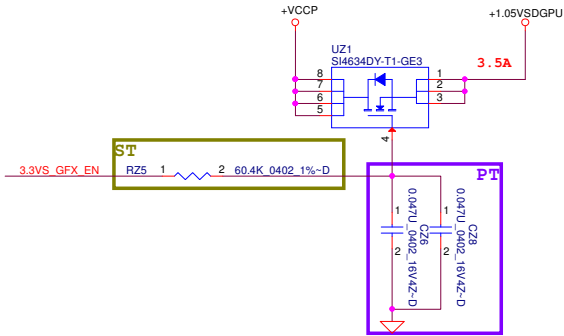
GB2-64, GB4-128	Channel 0 3-31	GB2-64, GB4-128	Channel 1 32-63
CW00	C3*	CW16	C3*
CW01	A2_BA3	CW17	A2_BA3
CW02	A2_BA0	CW18	A2_BA0
CW03	A4_BA3	CW19	A4_BA3
CW04	A5_BA1	CW20	A5_BA1
CW05	WE*	CW21	WE*
CW06	A7_AB	CW22	A7_AB
CW07	A6_A11	CW23	A6_A11
CW08	AB*	CW24	AB*
CW09	A12_BF1	CW25	A12_BF1
CW10	A6_A10	CW26	A6_A10
CW11	A1_A9	CW27	A1_A9
CW12	BA*	CW28	BA*
CW13	B0*	CW29	B0*
CW14	CX*	CW30	CX*
CW15	CAX*	CW31	CAX*



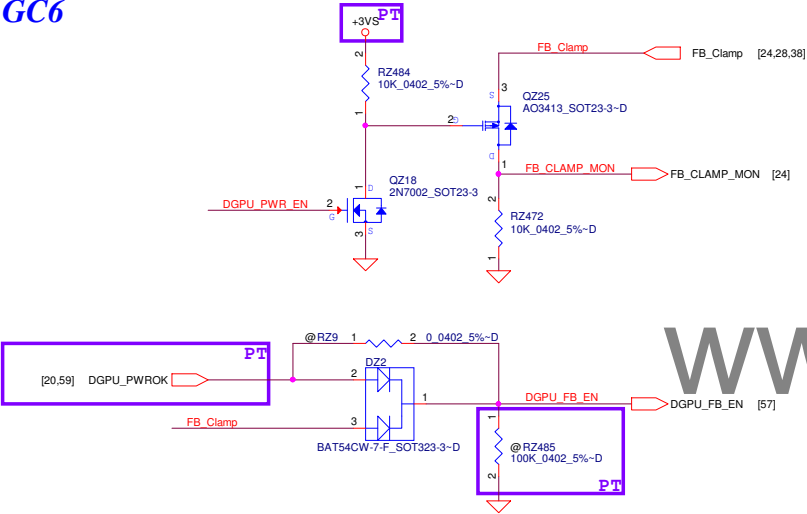
www.aitech1.ru

Security Classification	Compal Secret Data		Compal Electronics, Inc. Block Diagram	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title Doc Number
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND UNPUBLISHED INFORMATION. THIS SHEET IS NOT TO BE REPRODUCED FROM THE CUSTODY OF THE COMPANY OR FROM ANY OTHER PARTY WITHOUT PERMISSION OF COMPAL ELECTRONICS, INC. NO PART OF THIS SHEET OR THE INFORMATION CONTAINED HEREIN MAY BE REPRODUCED OR TRANSMITTED IN ANY FORM OR BY ANY MEANS, ELECTRONIC OR MECHANICAL, INCLUDING PHOTOCOPYING, RECORDING, OR BY ANY INFORMATION STORAGE AND RETRIEVAL SYSTEM, WITHOUT THE WRITTEN PERMISSION OF COMPAL ELECTRONICS, INC.			Date: Tuesday, September 03, 2013 10:56 AM 32 of 31	

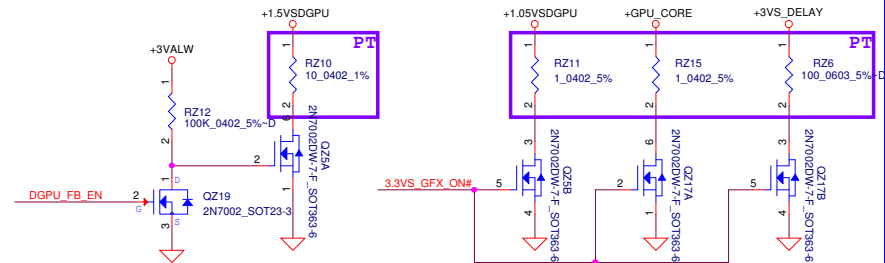
+1.05VS to +1.05VSDGPU



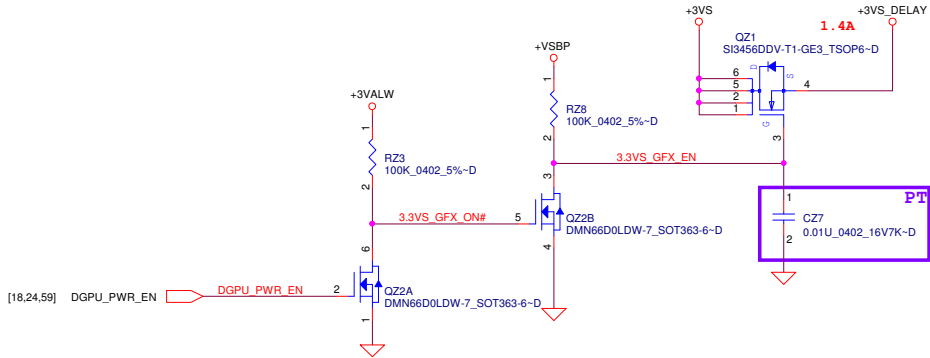
GC6



Discharge



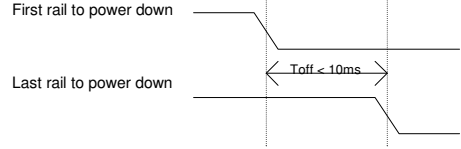
+3VS to +3VS_DELAY



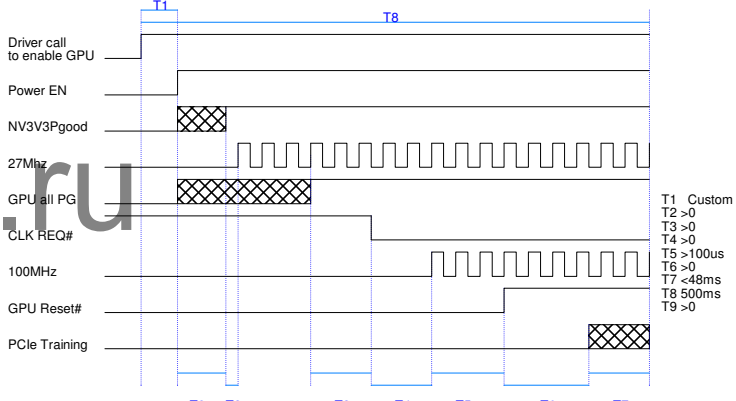
GPU Power Up Power Rail Sequence



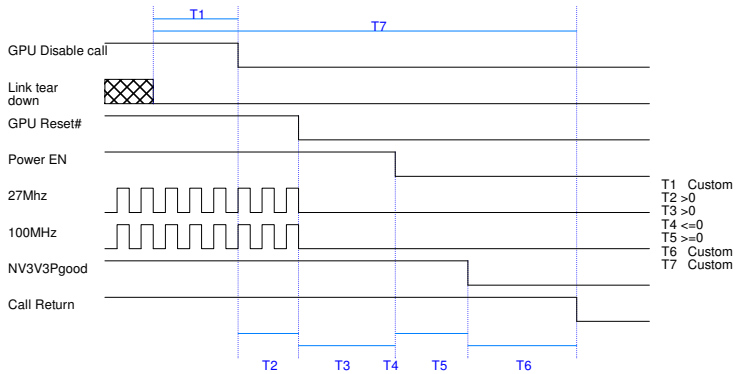
GPU Power Down Sequence



GPU Power Up Sub-system Sequence

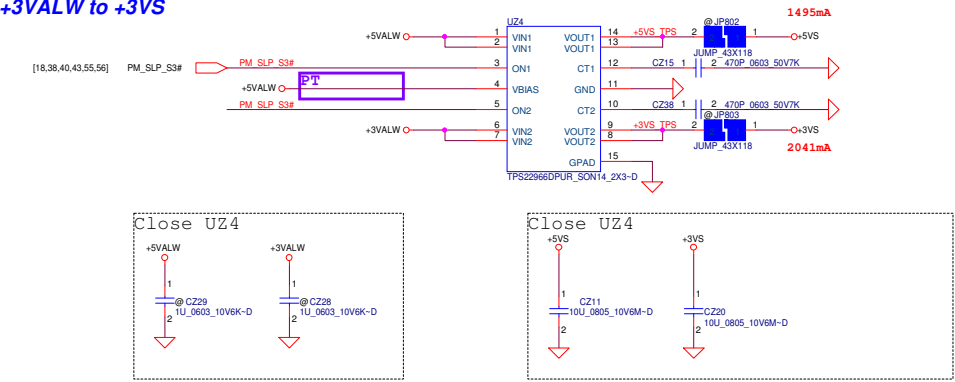


GPU Power Down Sub-system Sequence

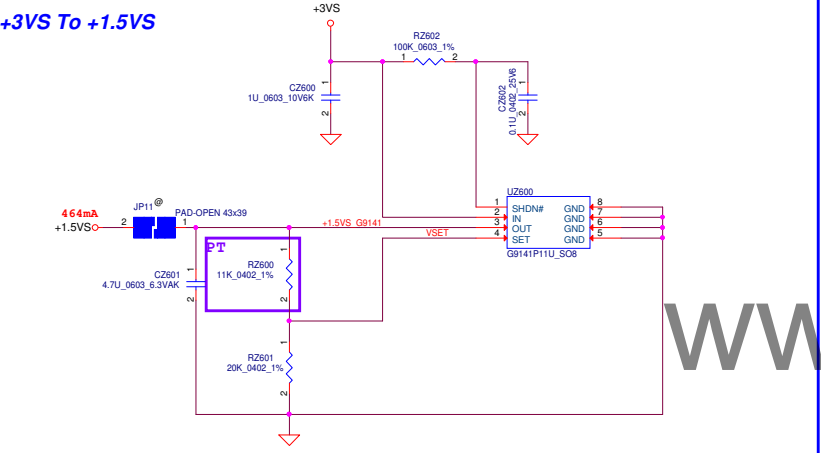


Security Classification	Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Block Diagram	Rev 0.1
			Date: Tuesday, September 03, 2013	Sheet 33 of 62

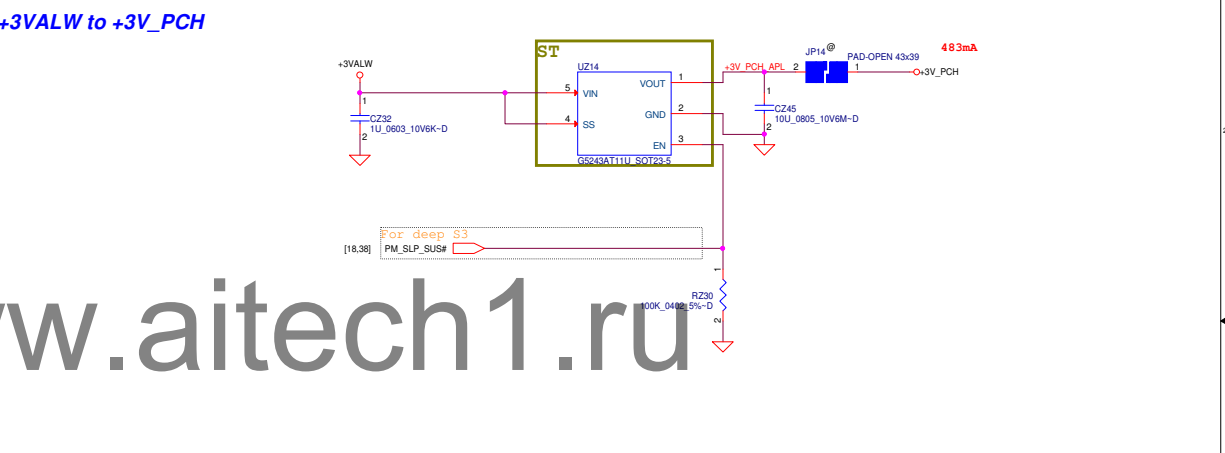
+5VALW to +5VS
+3VALW to +3VS



+3VS To +1.5VS



+3VALW to +3V_PCH



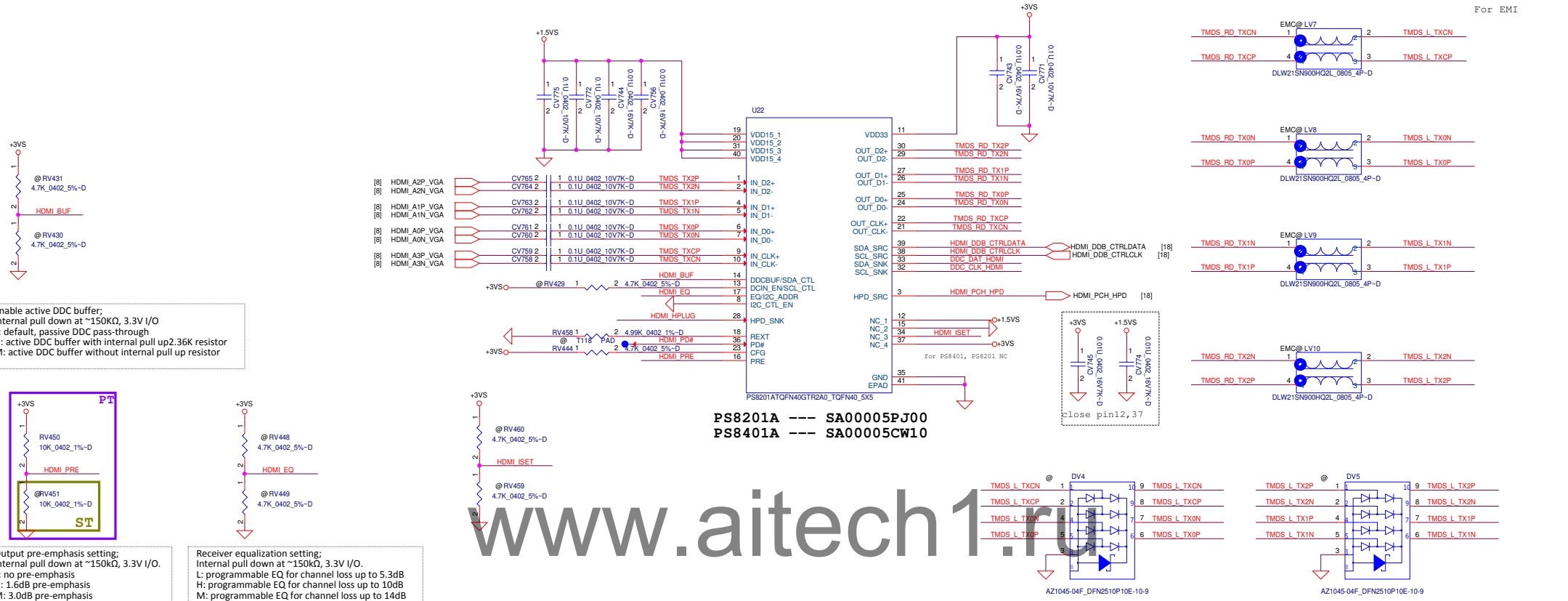
www.aitech1.ru

Discharge

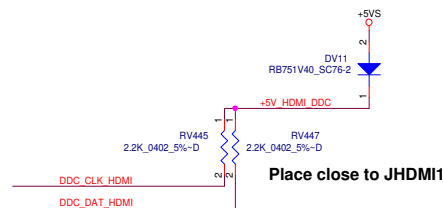
HDMI Active Level Shift (ALS type)

Place close to JHDMI1

For EMI

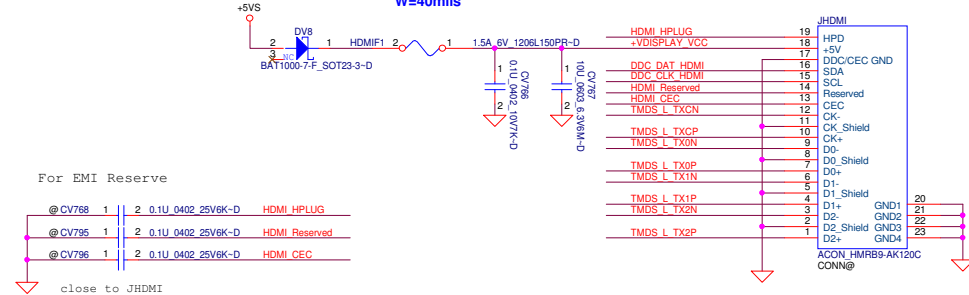


HDMI DDC

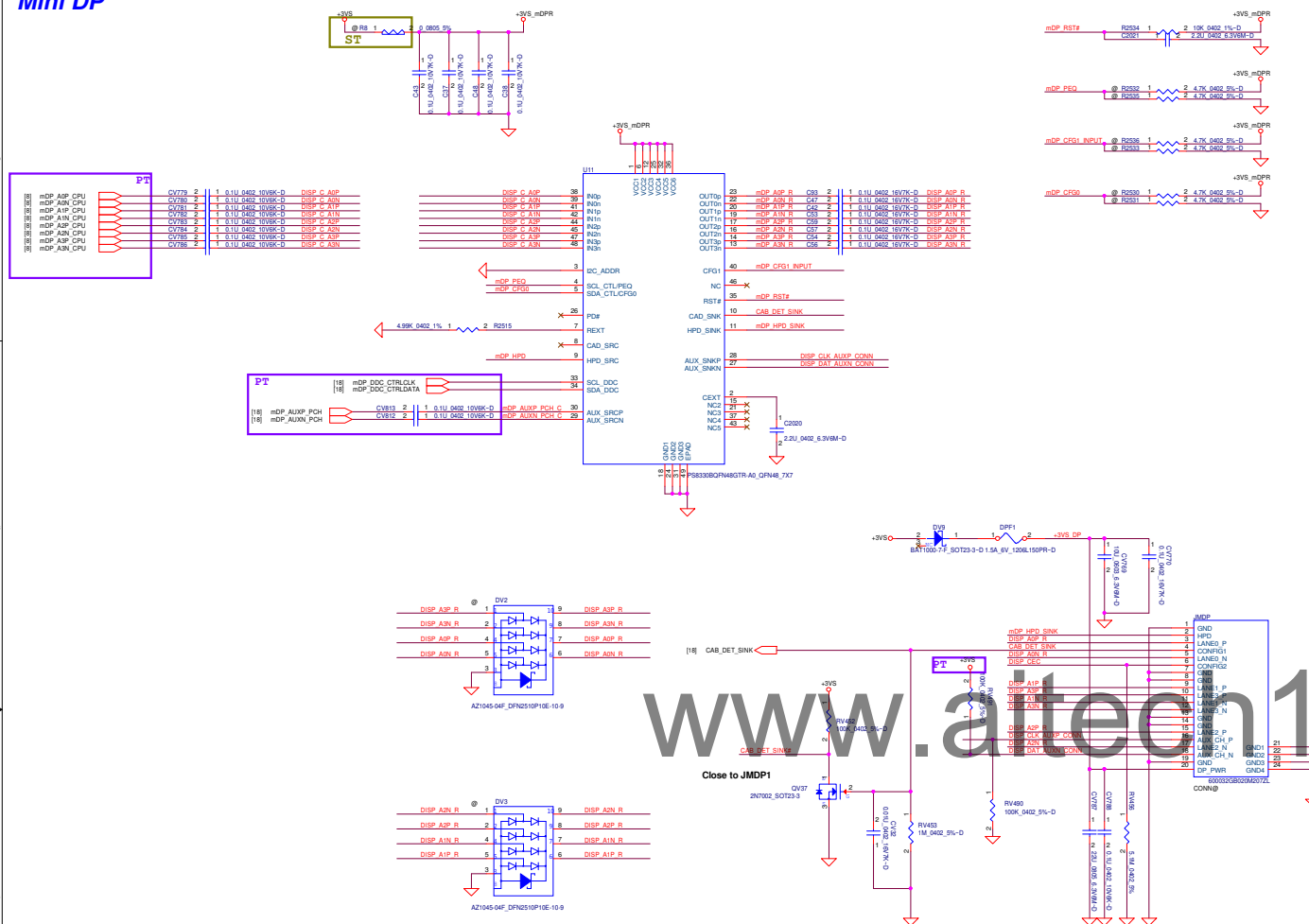


HDMI conn

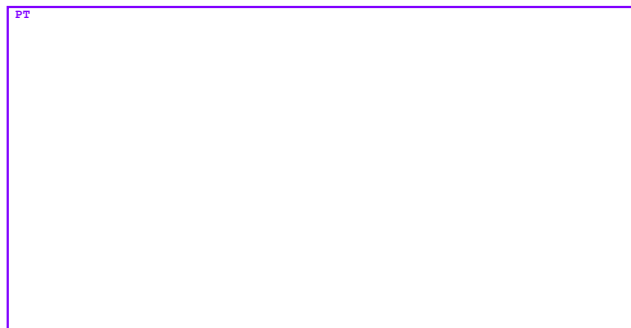
W=40mils



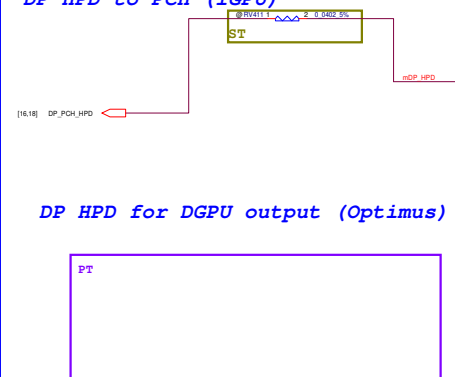
Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				HDMI		
				Size	Document Number	Rev
					LA-7851P	0
				Date:	Tuesday, September 03, 2013	Sheet 36 of 62

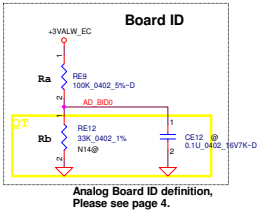
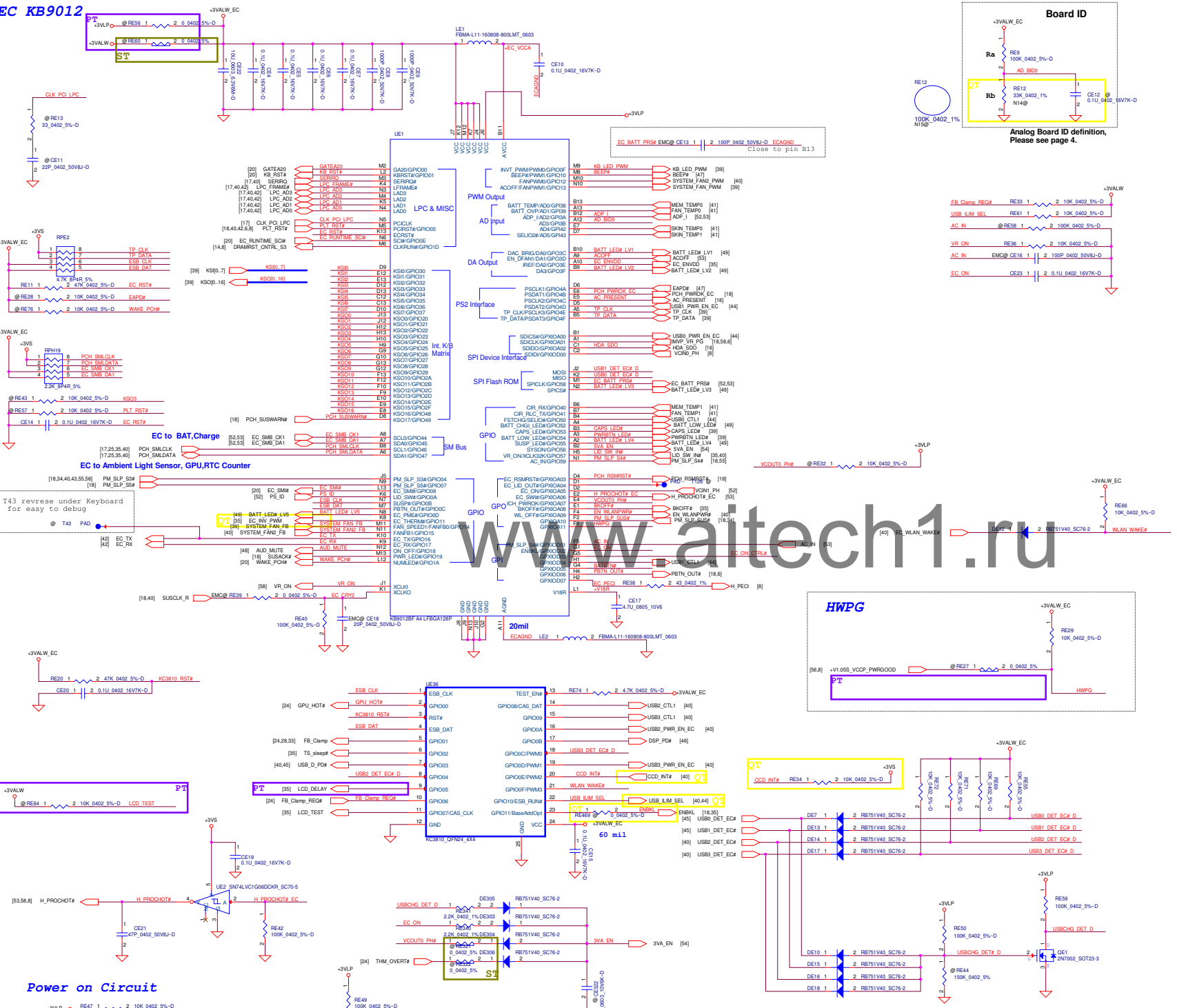


DDC Dongle SW for DP

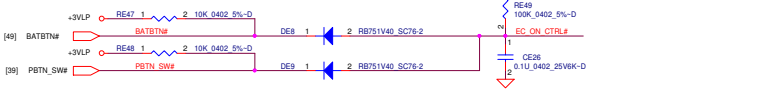


DP HPD to PCH (iGPU)



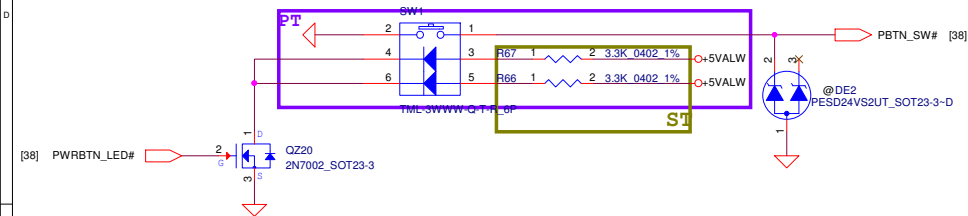


Power on Circuit

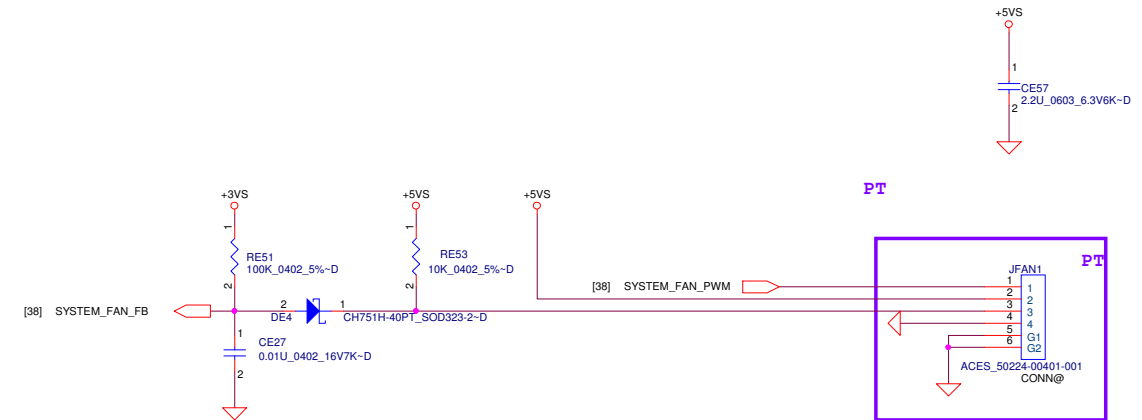


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2015/07/25	Title	EC ENE-KB930/ ENE3810
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Rev 0.1
Size	Document Number	LA-7851P		Date	Tuesday, September 17, 2013
		Sheet		38 of 62	

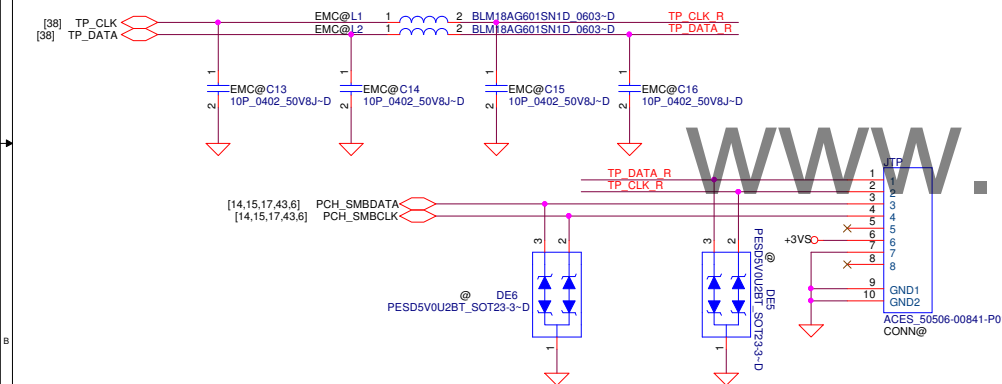
Power on Button



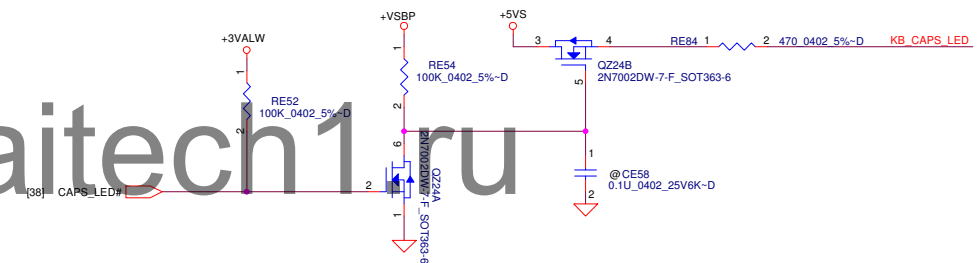
PWM FAN



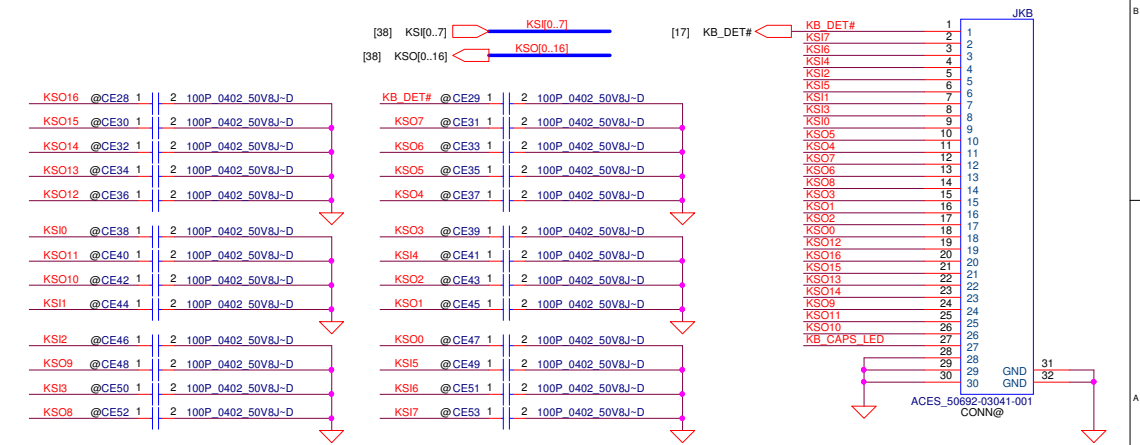
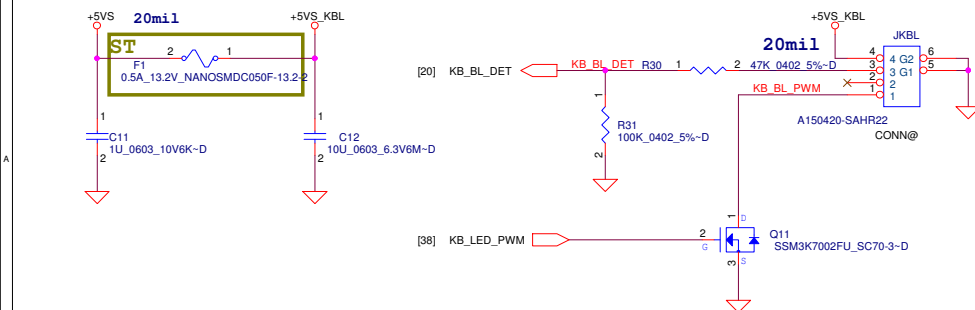
Touch pad



INT_KBD CONN

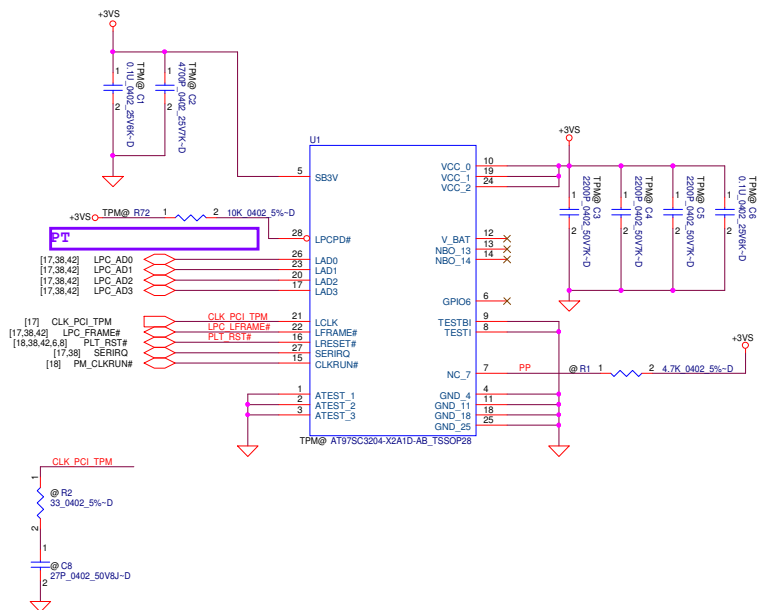


Keyboard back light

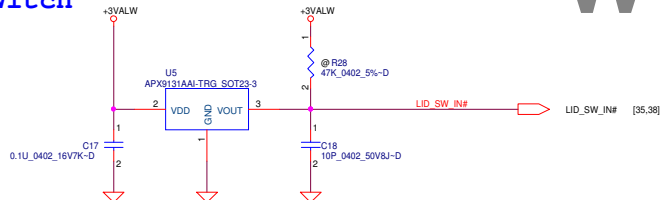


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	SW/TP/SCREW	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF FURTHERMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	Rev	
				LA-7851P	0.1	
				Date	Tuesday, September 03, 2013	Sheet

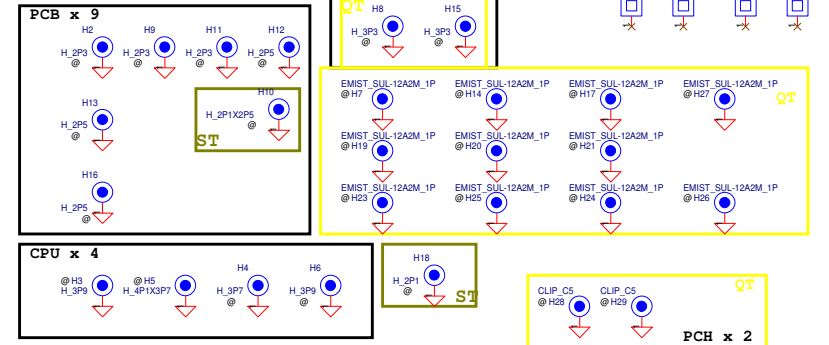
ATMEL TPM



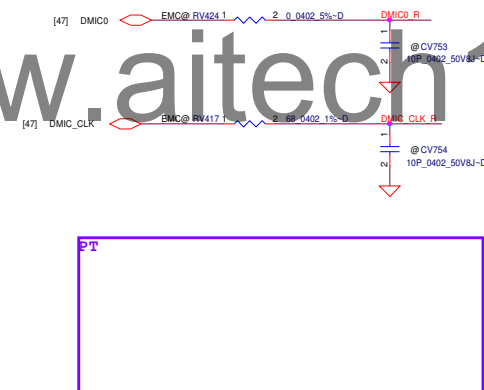
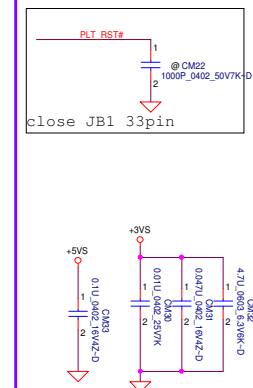
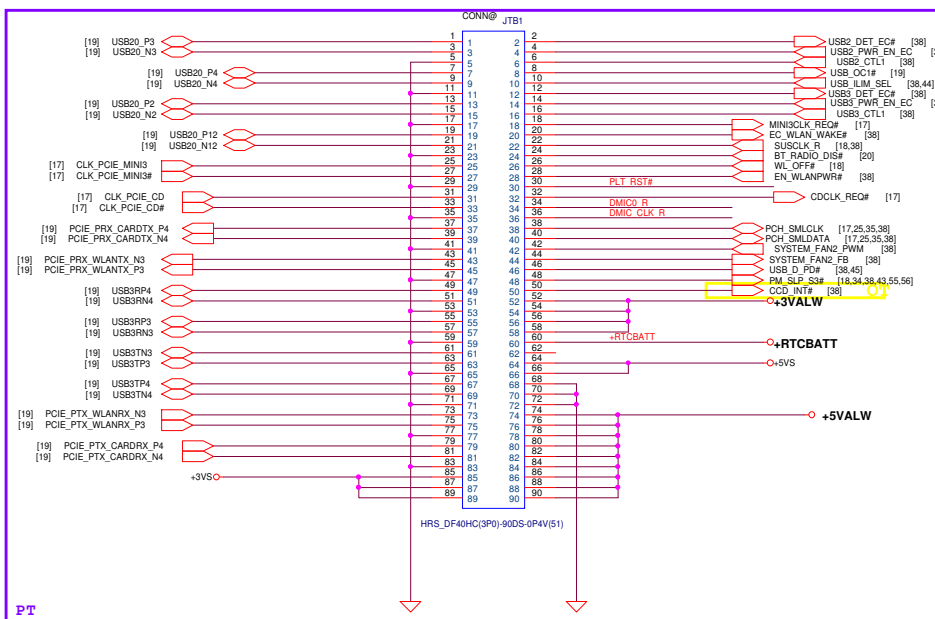
Lid Switch



Screw Hole



M/B to D/B conn.



Wedcam PWR CTRL

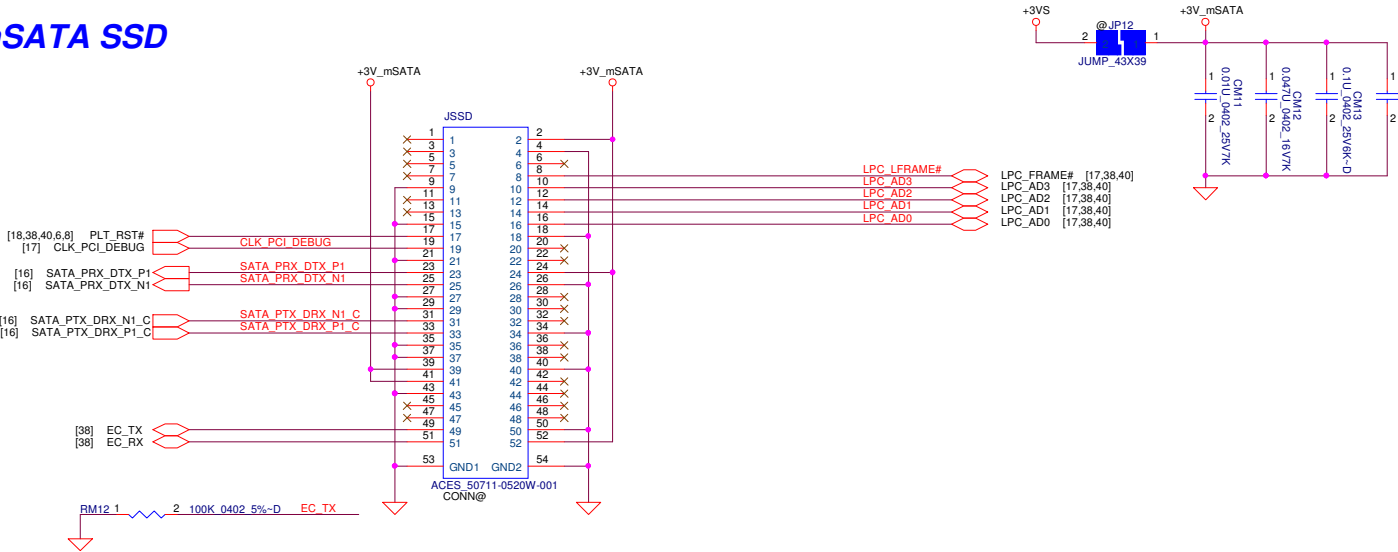


Security Classification		Compal Secret Data		Compal Electronics, Inc.		
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title		
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				CONN & LID		
				Size	Document Number	Rev.
				LA-7851P		
Date:				Thursday, September 05, 2013	Sheet	40 of 62

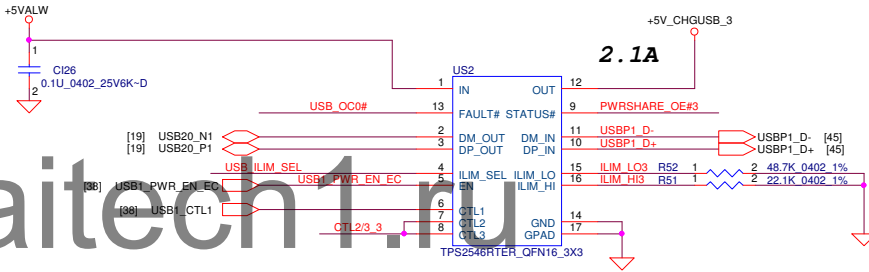
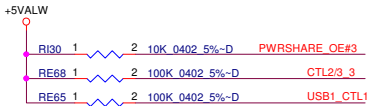
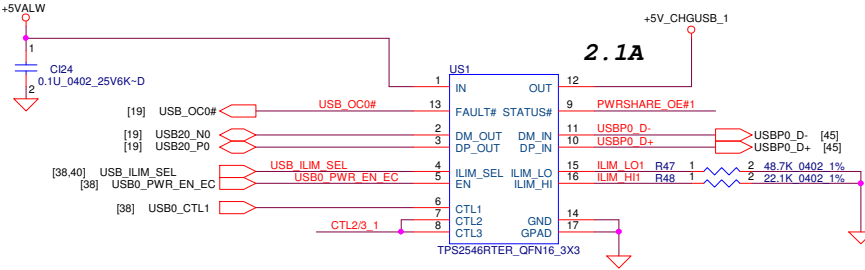
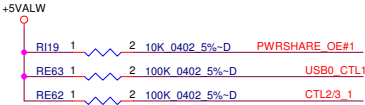
www.aitech1.ru

Pin#	Assignment	Description	Pin#	Assignment	Description
1	N/A	N/A	27	GND	Return Current Path
2	+3.3V	3.3V source	28	N/A	N/A
3	N/A	N/A	29	GND	Return Current Path
4	GND	Return Current Path	30	N/A	N/A
5	N/A	N/A	31	-A (port 1)	SATA Differential RX+ based on SSD
6	N/A	N/A	32	N/A	N/A
7	N/A	N/A	33	+A (port 1)	SATA Differential RX+ based on SSD
8	N/A	N/A	34	GND	Return Current Path
9	GND	Return Current Path	35	GND	Return Current Path
10	N/A	N/A	36	Reserved	No Connect
11	N/A	N/A	37	GND	Return Current Path
12	N/A	N/A	38	Reserved	No Connect
13	N/A	N/A	39	+3.3V	3.3V Source
14	N/A	N/A	40	GND	Return Current Path
15	GND	Return Current Path	41	+3.3V	3.3V Source
16	N/A	N/A	42	N/A	N/A
17	N/A	N/A	43	N/A	N/A
18	GND	Return Current Path	44	N/A	N/A
19	N/A	N/A	45	Reserved	N/A
20	N/A	N/A	46	N/A	N/A
21	GND	Return Current Path	47	Reserved	N/A
22	N/A	N/A	48	N/A	N/A
23	+B(port 1)	SATA Differential	49	DA/DSO	Device Activity / Disable Staggered Spin-up
24	+3.3V	3.3V Source	50	GND	Return Current Path
25	-B(port 1)	SATA Differential	51	Presence Detection	Shall be pulled to GND by device
26	GND	Return Current Path	52	+3.3V	3.3V Source

mSATA SSD

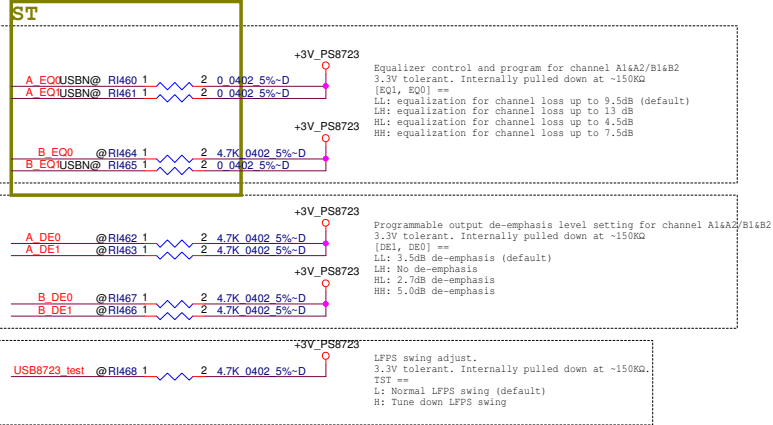
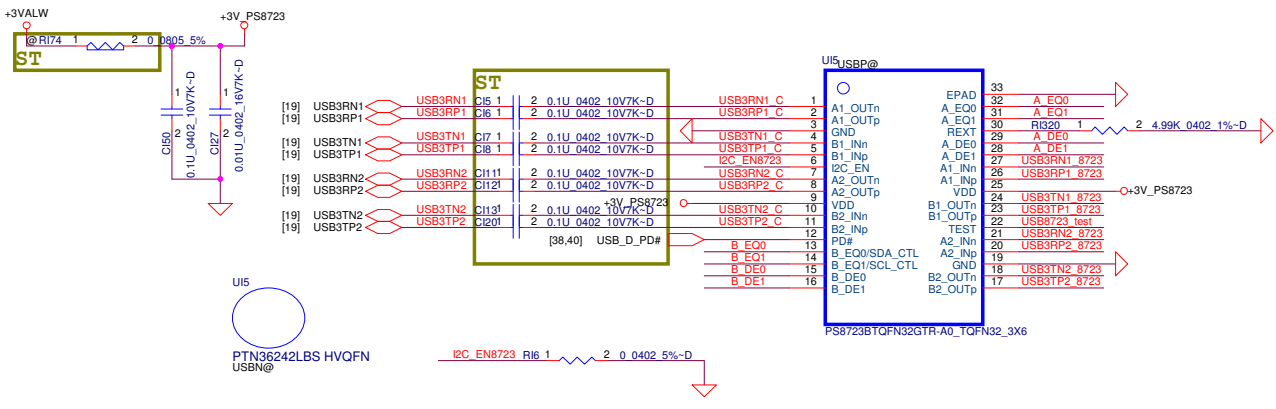


USB Powershare

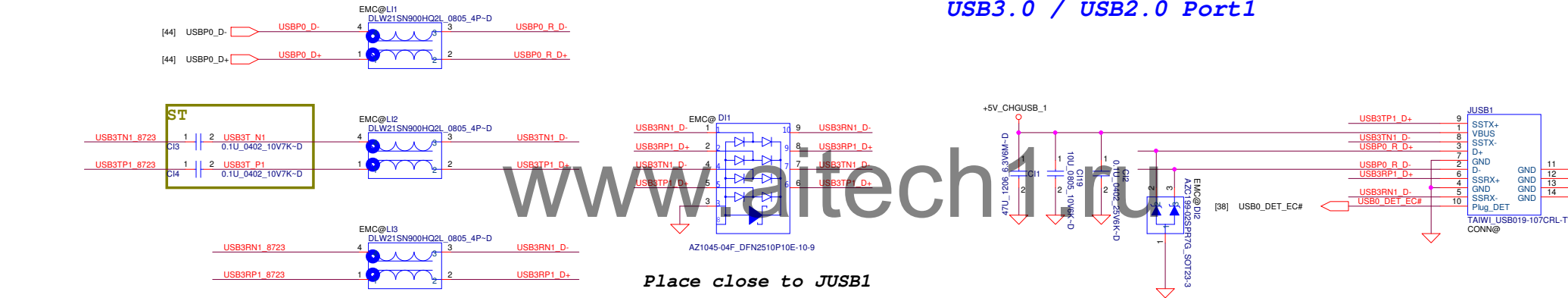


www.aitech1.ru

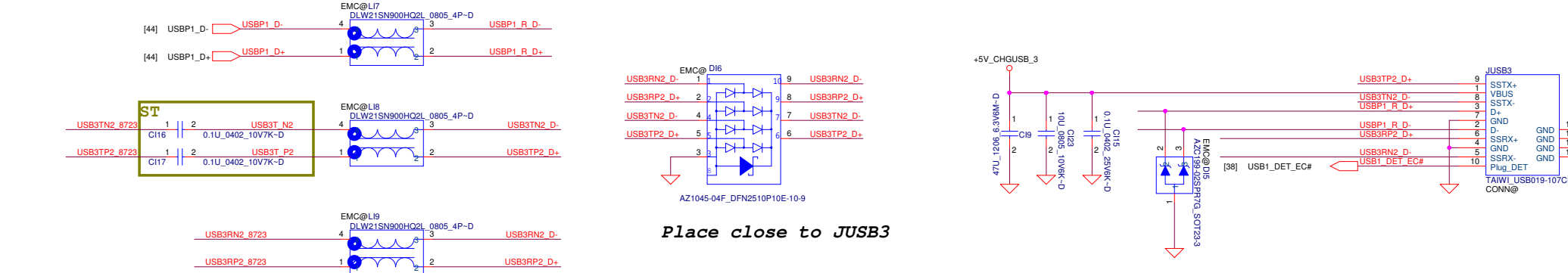
USB3.0 Re-driver



USB3.0 / USB2.0 Port1

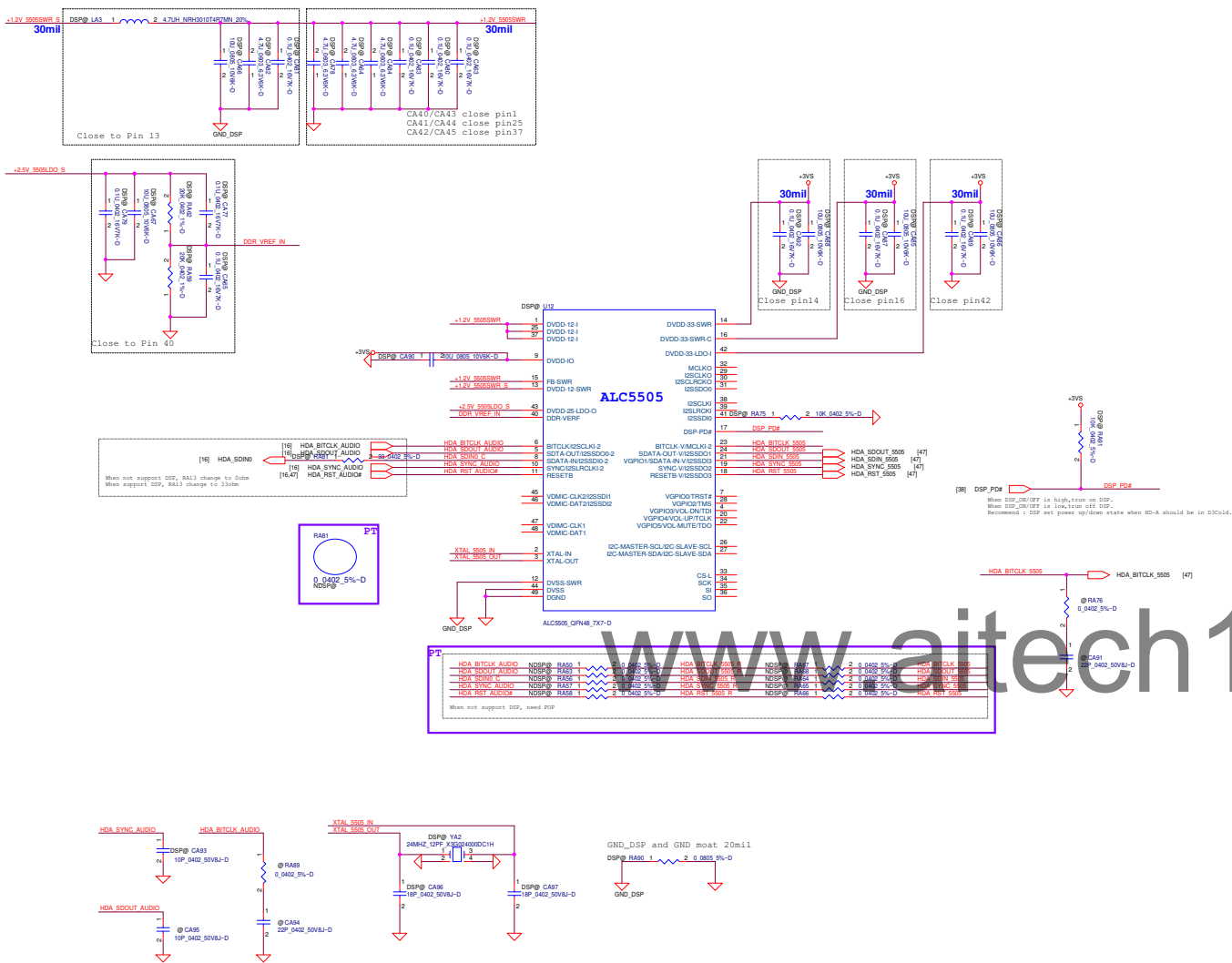


USB3.0 / USB2.0 Port3



Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	Title	
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				USB conn.	
				LA-7851P	
				Date: Tuesday, September 03, 2013	
				Sheet 45 of 62	
				Rev 0.1	

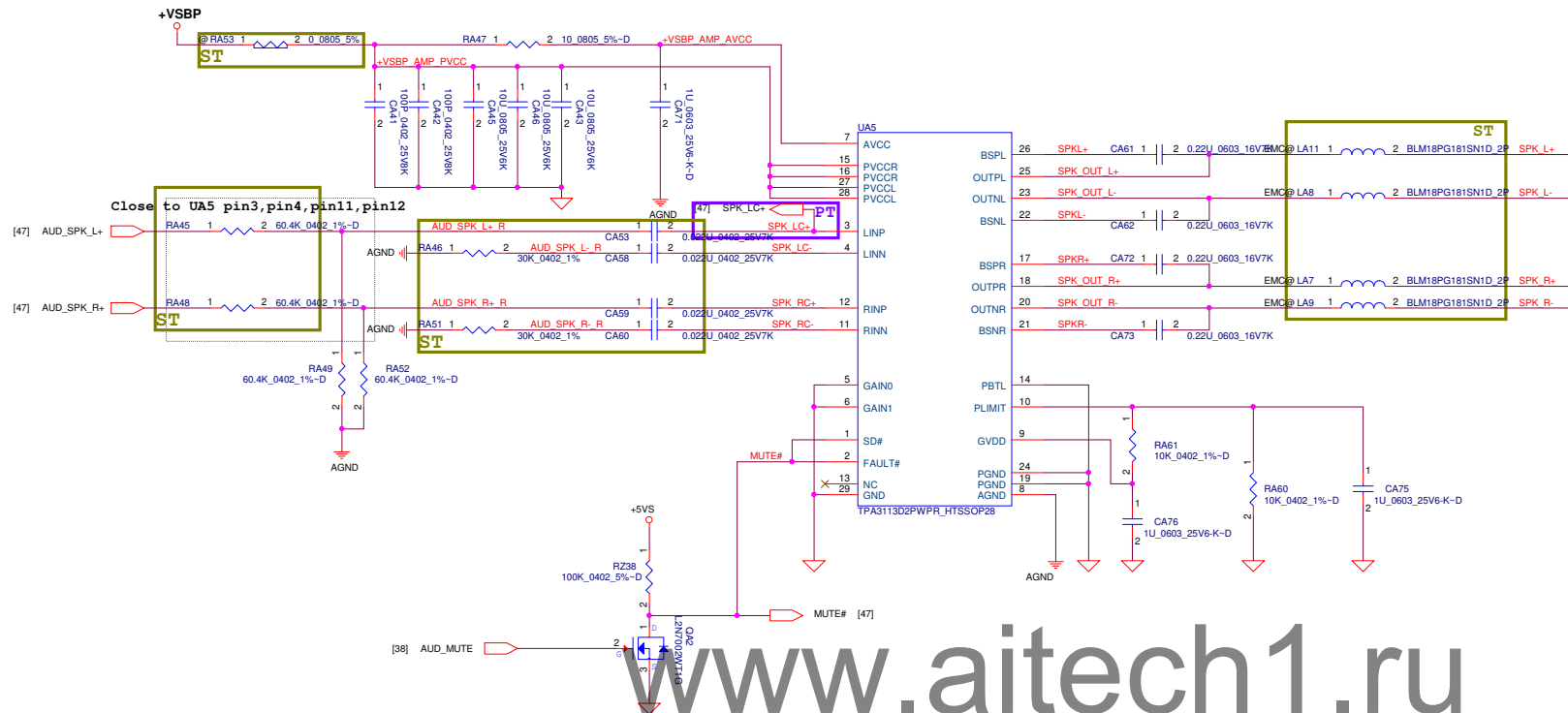
HD Audio DSP



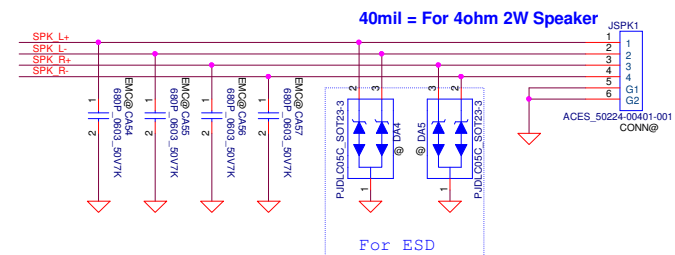
Green Clock

Security Classification	Compel Secret Data		Title	Compel Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/25	RTC Counter/Green Clock	
THIS SHEET OF ENGINEERING DRAWINGS IS THE PROPRIETARY PROPERTY OF COMPTEL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D TO ANY OTHER DIVISION OR AUTHORIZED BY COMPTEL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPTEL ELECTRONICS, INC. MAY BE USED OR BY DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPTEL ELECTRONICS, INC.			Size	Document Number	Rev
			Udate	Wednesday, September 04, 2013	Sheet 46 of 82

Audio AMP

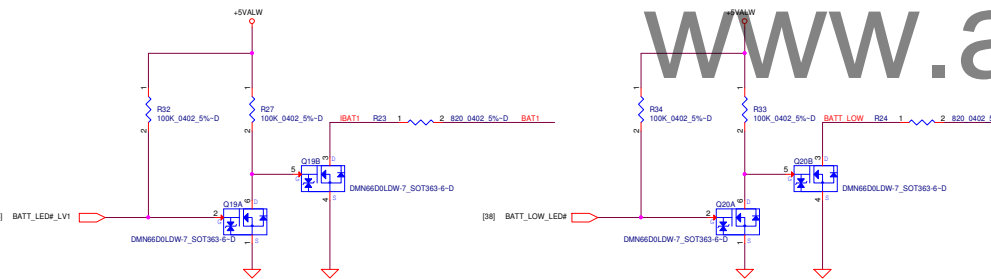
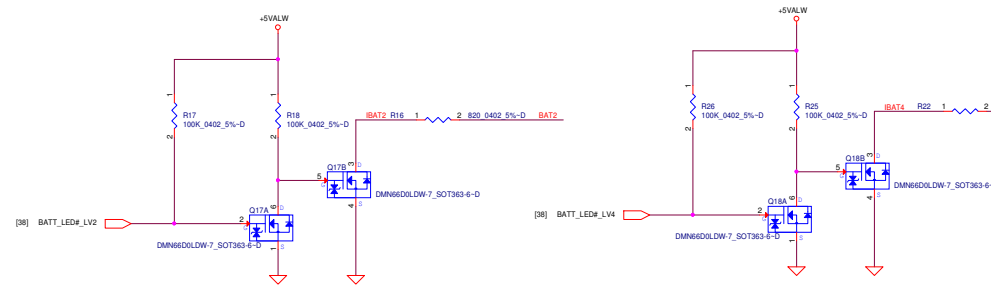
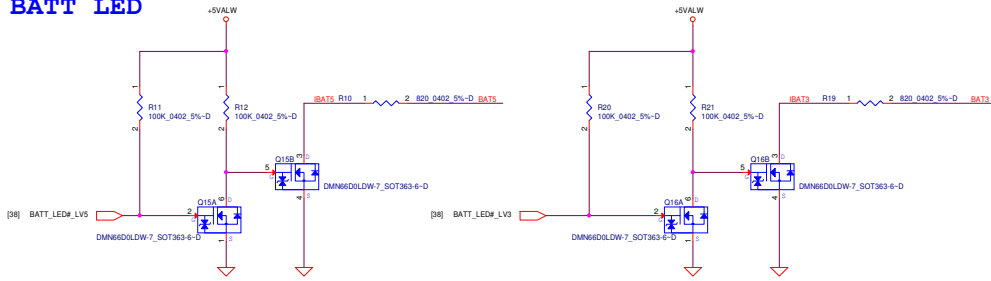


Int. Speaker Conn.

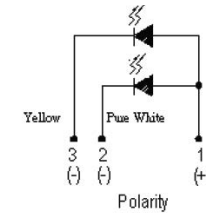
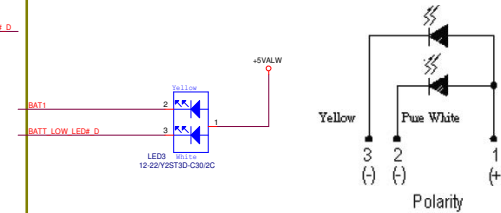
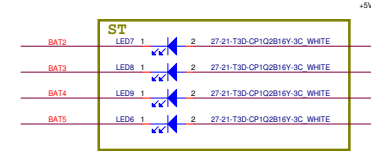
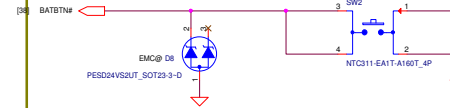


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/21	Title	Speaker/Audio Jack
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF RAISE TO ANY OTHER DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.				Document Number	LA-7851P
				Date	Tuesday, September 03, 2013
				Sheet	48 of 62

BATT LED

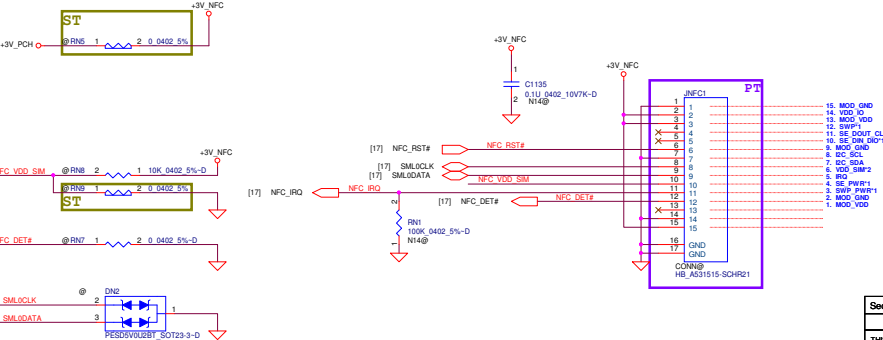


BATT LED Power Button



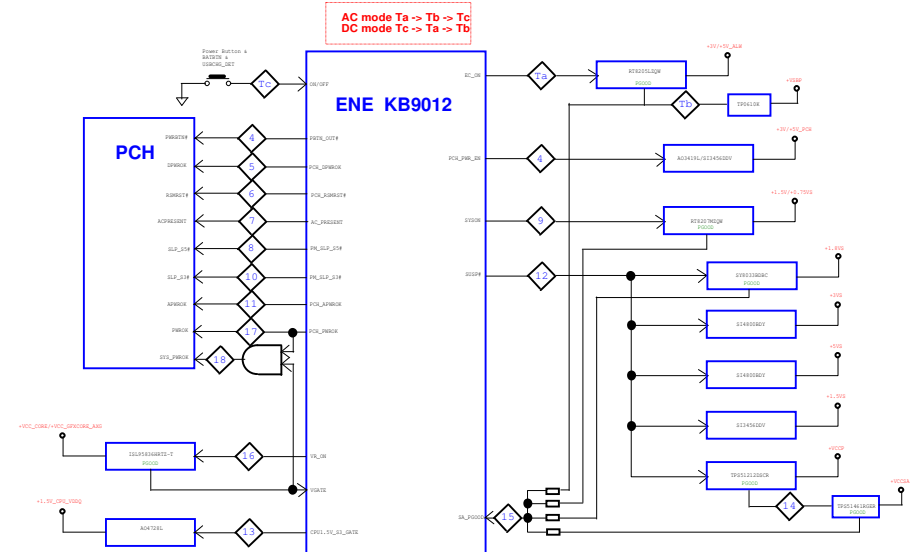
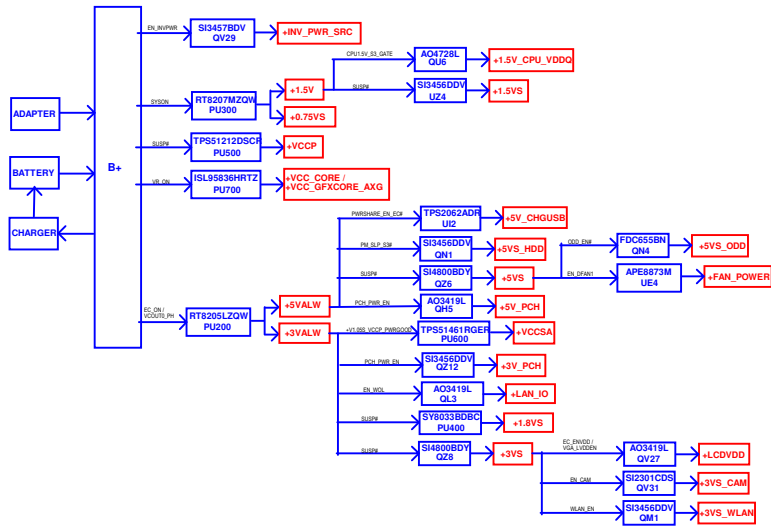
www.aitech1.ru

NFC Connector

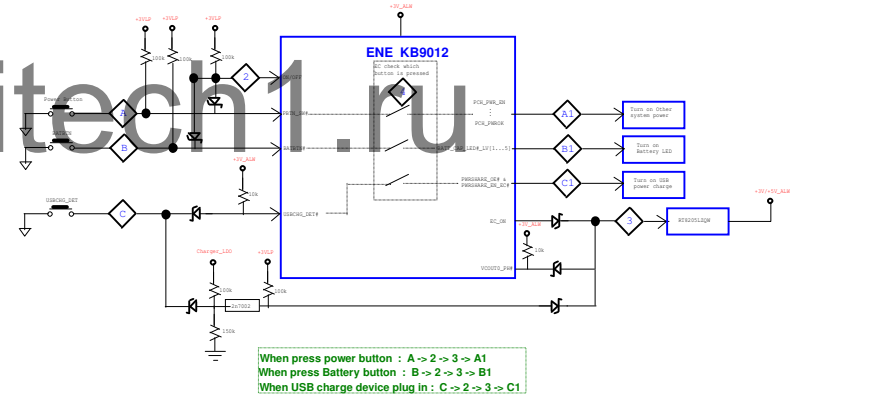
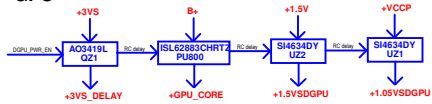


RTC counter

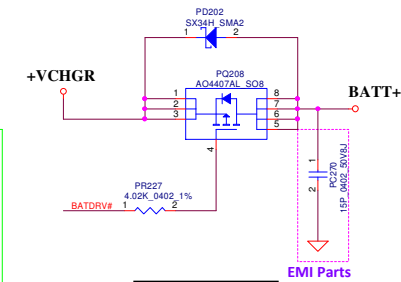
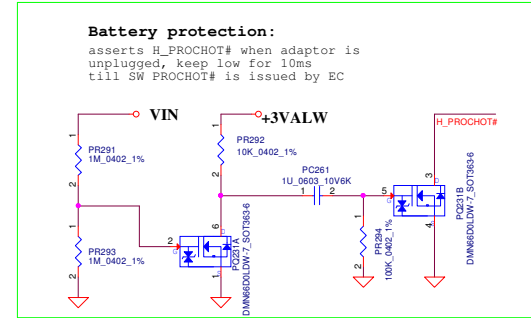
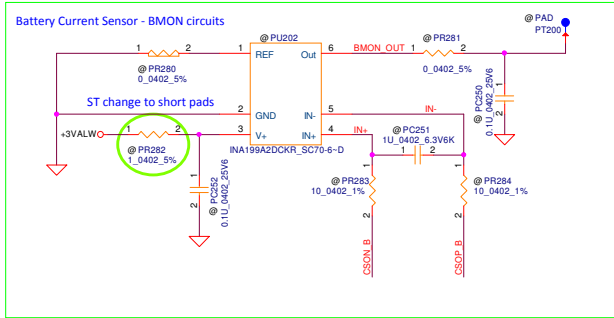
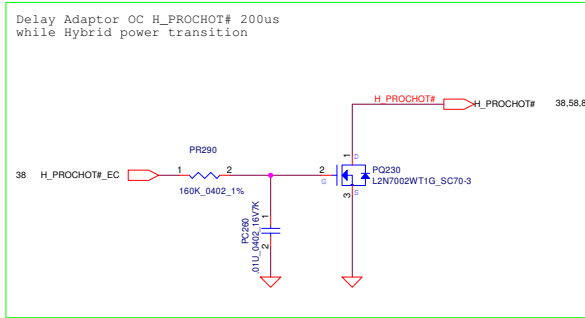
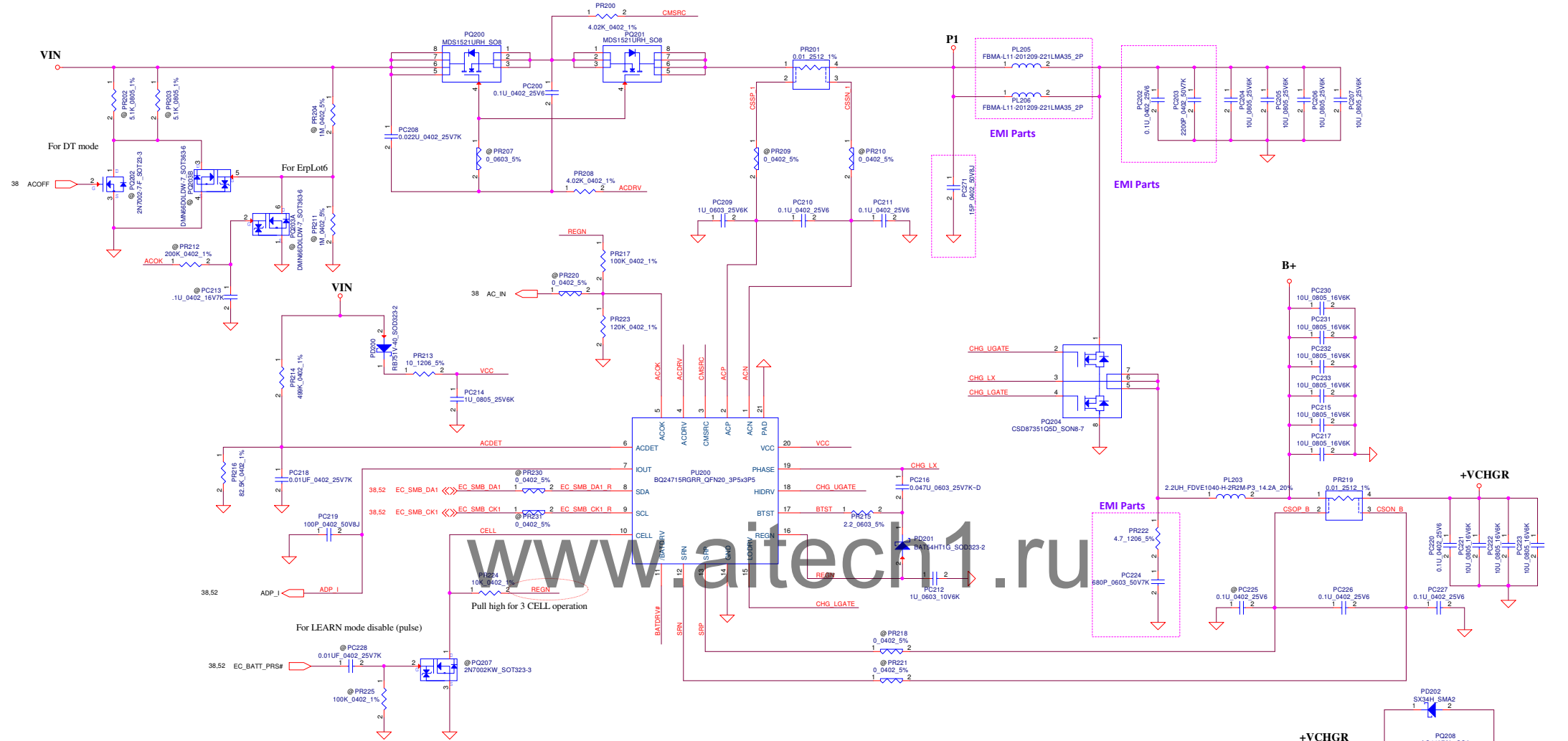
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2011/08/25	Deciphered Date	2012/07/15	Title	Speaker/Audio Jack
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.					Rev 0.1
Docum Number	LA-7841P				Date
Customer	Tuesday, September 17, 2013				Sheet 48 of 62



GPU

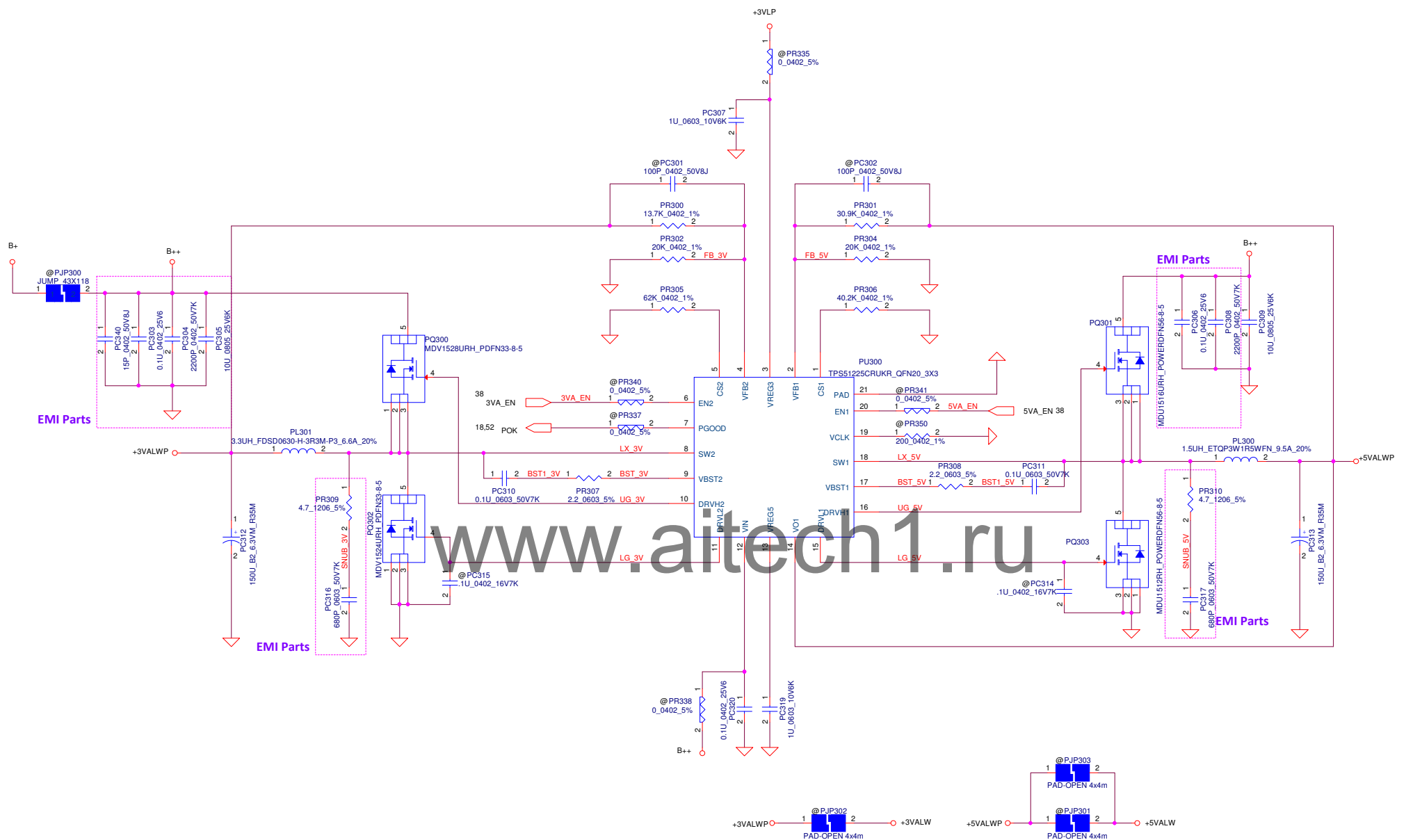


When press power button : A -> 2 -> 3 -> A1
When press Battery button : B -> 2 -> 3 -> B1
When USB charge device plug in : C -> 2 -> 3 -> C1



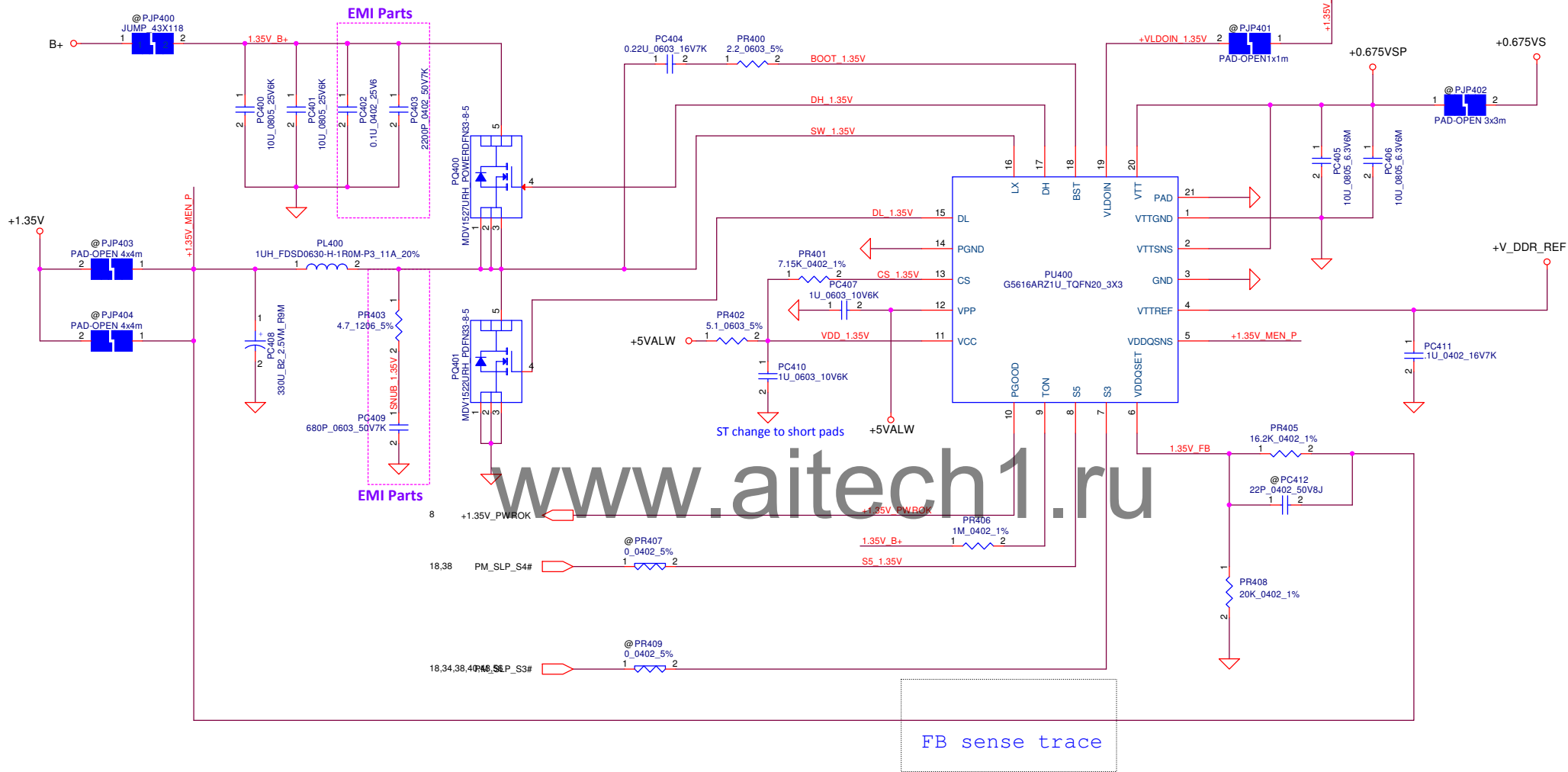
3S3P
CC = 5.28A
CV = 3S (12.6V)

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.



3.3VALWP
TDC 4.6A
Peak Current 6.5A
OCP current 7.8A

5VALWP
TDC 7.9A
Peak Current 11.3A
OCP current 13.4A



1.35V_{olt} +/- 5%
TDC 7.2A
Peak Current 10.2A
OCP current 12.2A

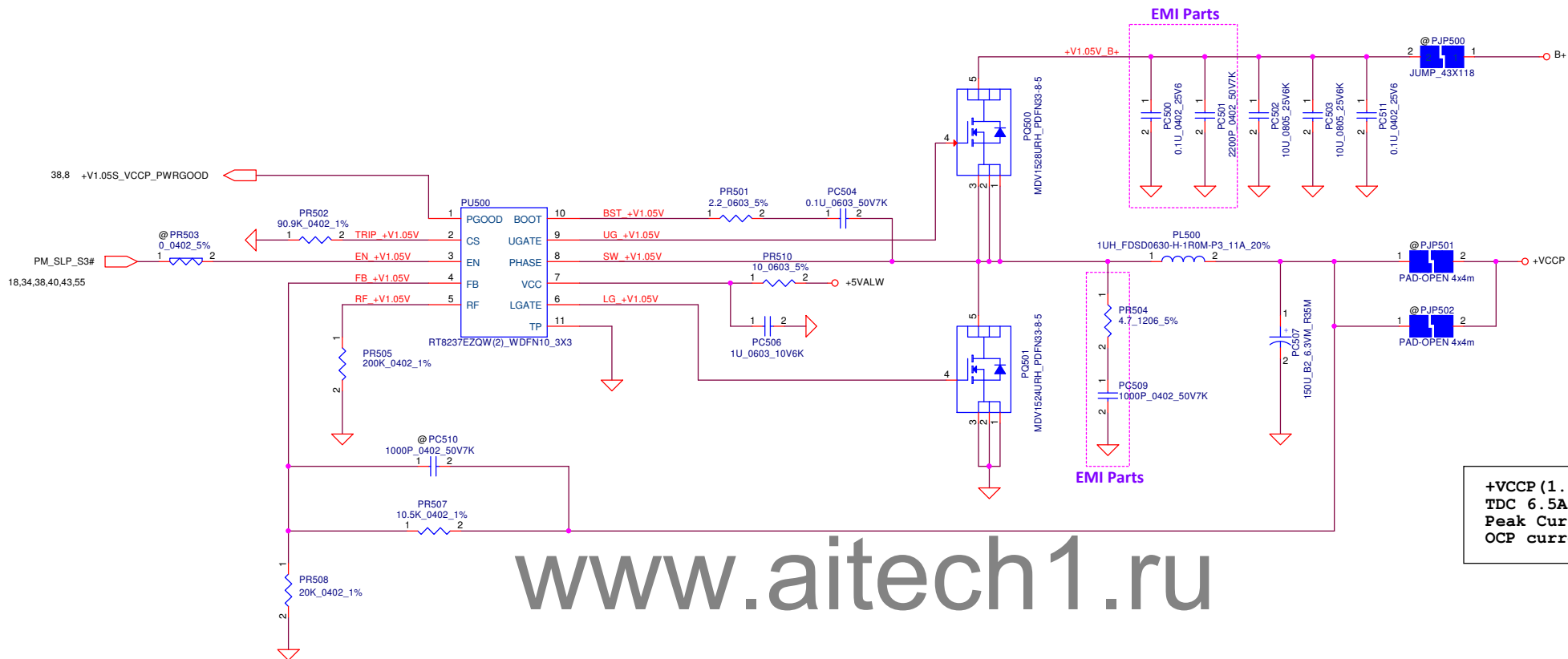
0.675V_{olt} +/- 5%
TDC 0.7A
Peak Current 1A
OCP Current 1.1A

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF COMPAL ELECTRONICS, INC. WITHOUT THE WRITTEN CONSENT OF COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



Compal Electronics, Inc.


Title		+1.35V MEN/+0.675V_DDR VTT	
Size	Document Number	LA-9941P	
Date	Thursday, September 05, 2013	Sheet	55 of 62
Rev	0.1		

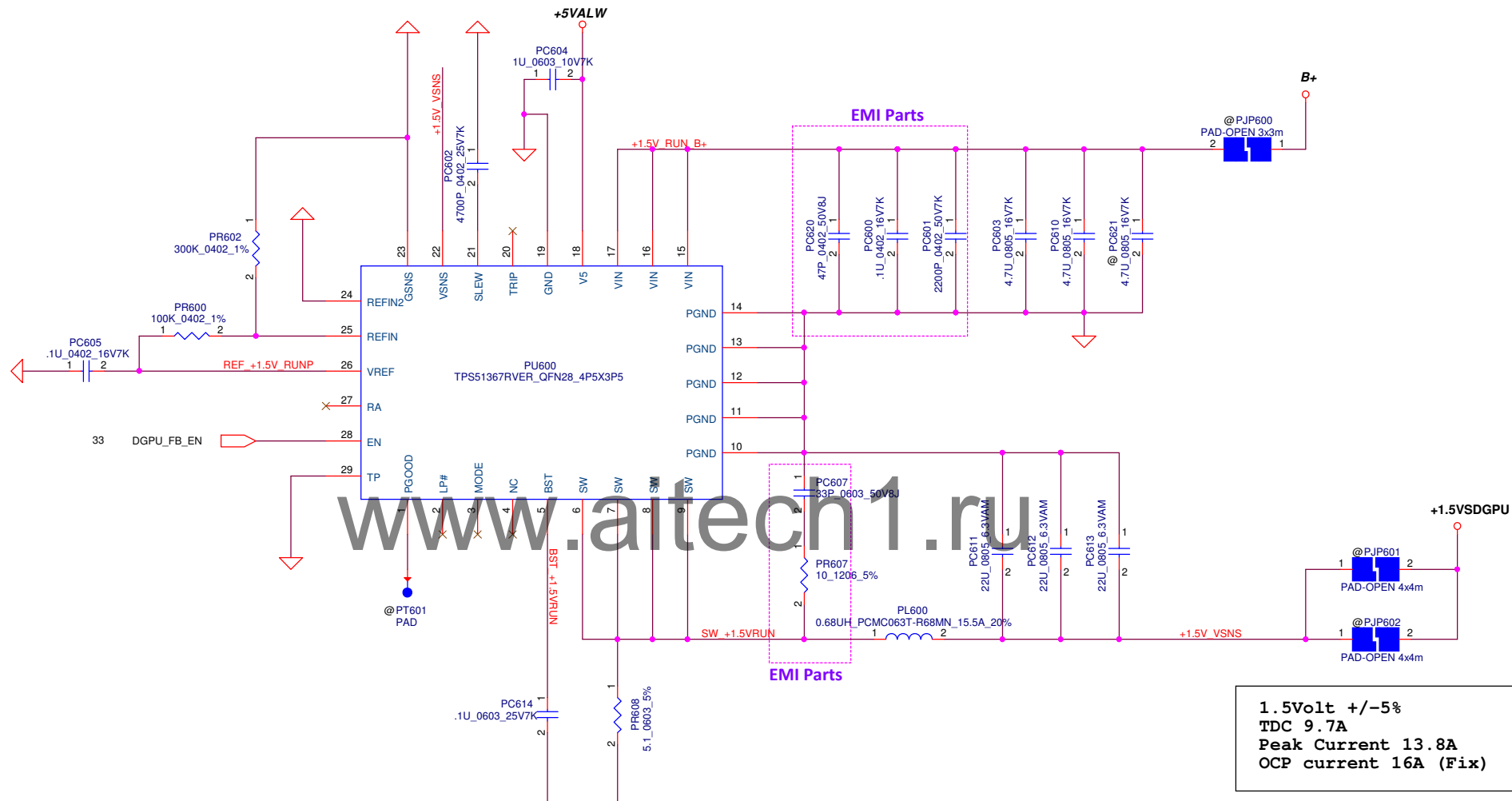


+VCCP (1.05V)
TDC 6.5A
Peak Current 9.2A
OCF current 11.1A

www.aitech1.ru

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL") THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

			
Compal Electronics, Inc.			
Title			
PWR-V1.05S_VCCPP			
Size			
Document Number			
LA-9941P			
Date			
Wednesday, September 04, 2013			
Sheet			
56 of 62			
Rev			
0.1			



DELL CONFIDENTIAL/PROPRIETARY

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OR DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



Compal Electronics, Inc.			
Title		PWR +1.5VRUN	
Size	Document Number	LA-9941P	
Date:	Wednesday, September 04, 2013	Sheet	57 of 62
		Rev	0.1

	TYP	MAX
H/S Rds (on) :	7.4mohm	8.1mohm
L/S Rds (on) :	2.6mohm	3.1mohm



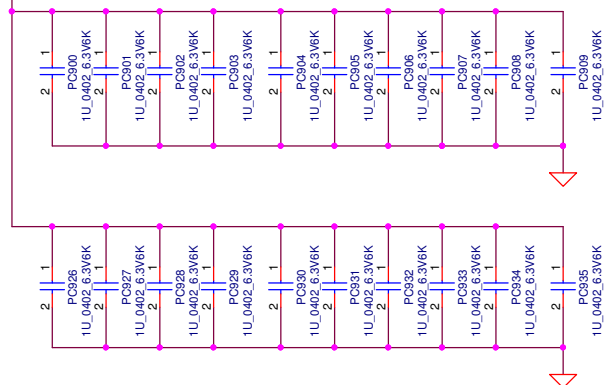
THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OR DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



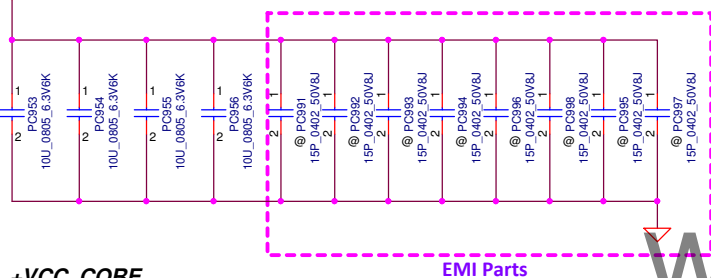
LA-9941P

Title			
VGA CORE			
Size	Document Number		Rev
	LA-9941P		0.1
Date:	Wednesday, September 04, 2013	Sheet	50 of 62

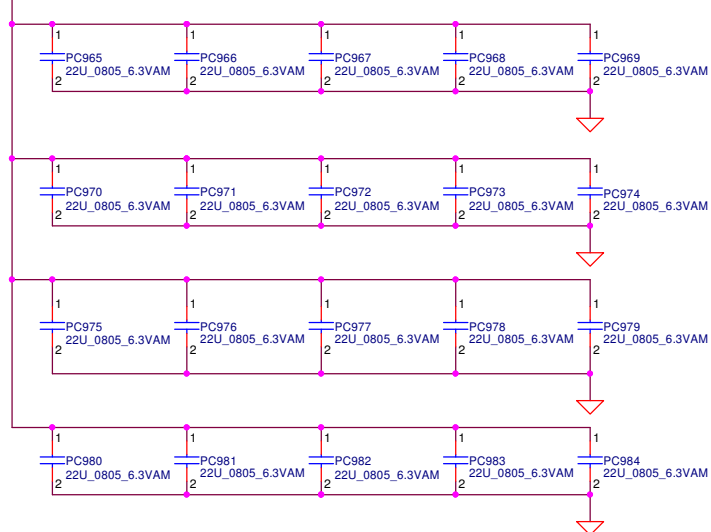
+VCC_CORE



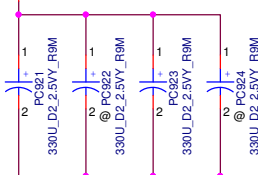
+VCC_CORE



+VCC_CORE



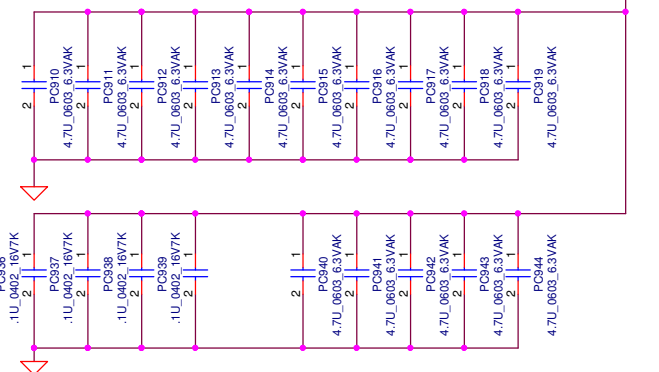
+VCC_CORE



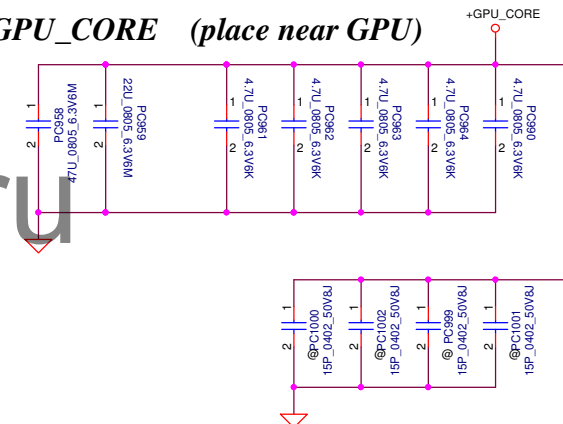
Based on PDDG
rev 1.1 Table 5-2.

Design guide:
+VCC_CORE
1. 470uF*4 (SGA0000420L)
2. 22uF*20 (SE000008L80)
3. 10uF*4 (SE160106M8L)
4. 1uF*20 (SE000000K8L)

+GPU_CORE (place under GPU)



+GPU_CORE (place near GPU)



Under:
1. 4.7uF*10 (SE000008L80)
2. 0.1uF*4 (SE160106M8L)
Near:
1. 4.7uF*5 (SE093475K80)
2. 22uF*1 (SE000001120)
3. 47uF*1 (SE000000PL0L)
4. 33uF*1 (SGA20331E10)

DELL CONFIDENTIAL/PROPRIETARY



Compal Electronics, Inc.

PROCESSOR DECOUPLING

Size Document Number

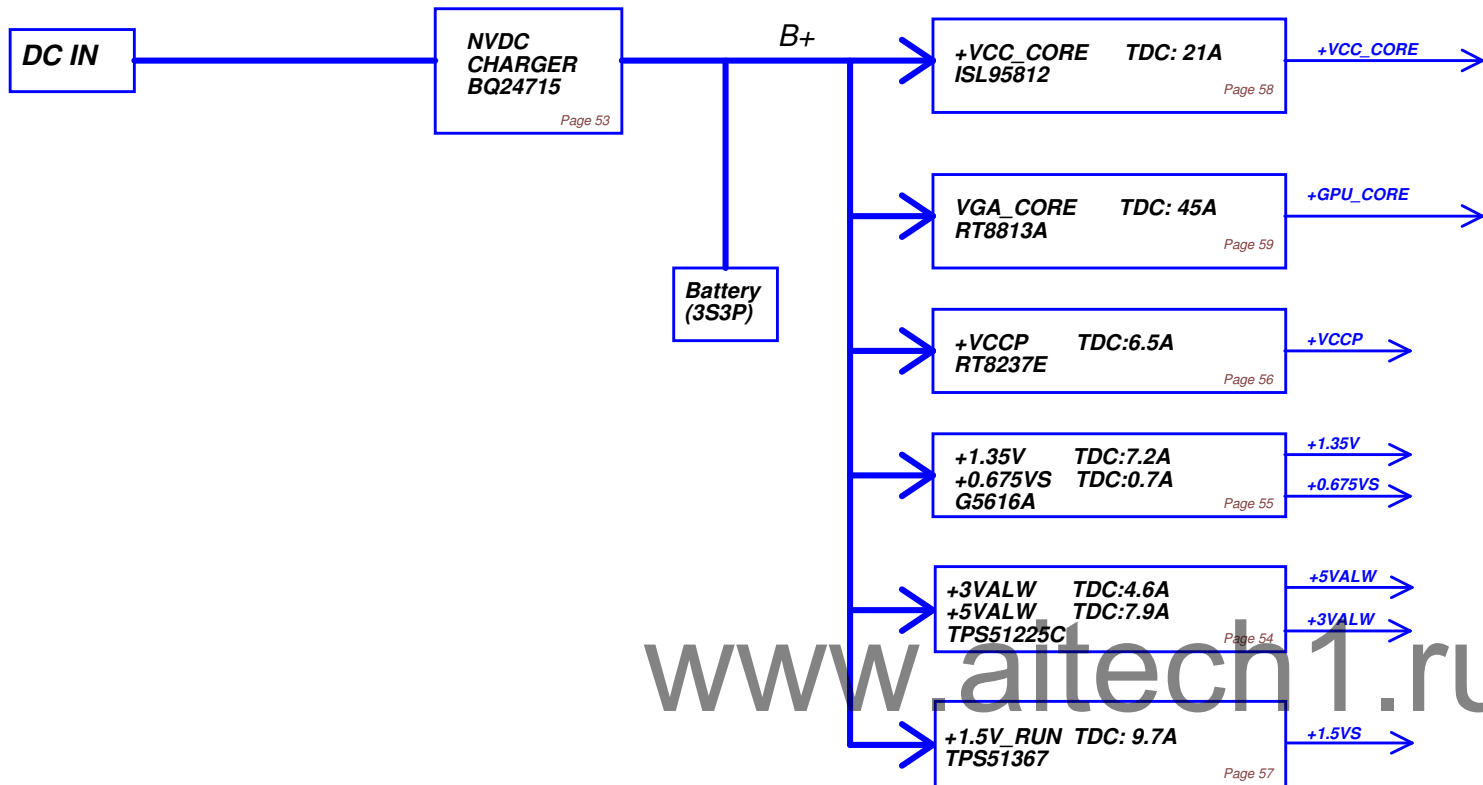
LA-9941P

Rev 0.1

Date: Wednesday, September 04, 2013


Sheet 60 of 62

THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.



www.aitech1.ru

PROPRIETARY NOTE: THIS SHEET OF ENGINEERING DRAWING AND SPECIFICATIONS CONTAINS CONFIDENTIAL, TRADE SECRET AND OTHER PROPRIETARY INFORMATION OF DELL INC. ("DELL"). THIS DOCUMENT MAY NOT BE TRANSFERRED OR COPIED WITHOUT THE EXPRESS WRITTEN AUTHORIZATION OF DELL. IN ADDITION, NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT DELL'S EXPRESS WRITTEN CONSENT.

		Compal Electronics, Inc.	
Title		POWER BLOCK DIAGRAM	
Size	Document Number	Rev	
	LA-9391P	0.1	
Date:	Wednesday, September 04, 2013	Sheet	61 of 62

